



Testing the Limits
FOR PRODUCT SUCCESS

Towards the Test Compaction of RF/AMS Integrated Systems Utilizing Novel Sensor Designs

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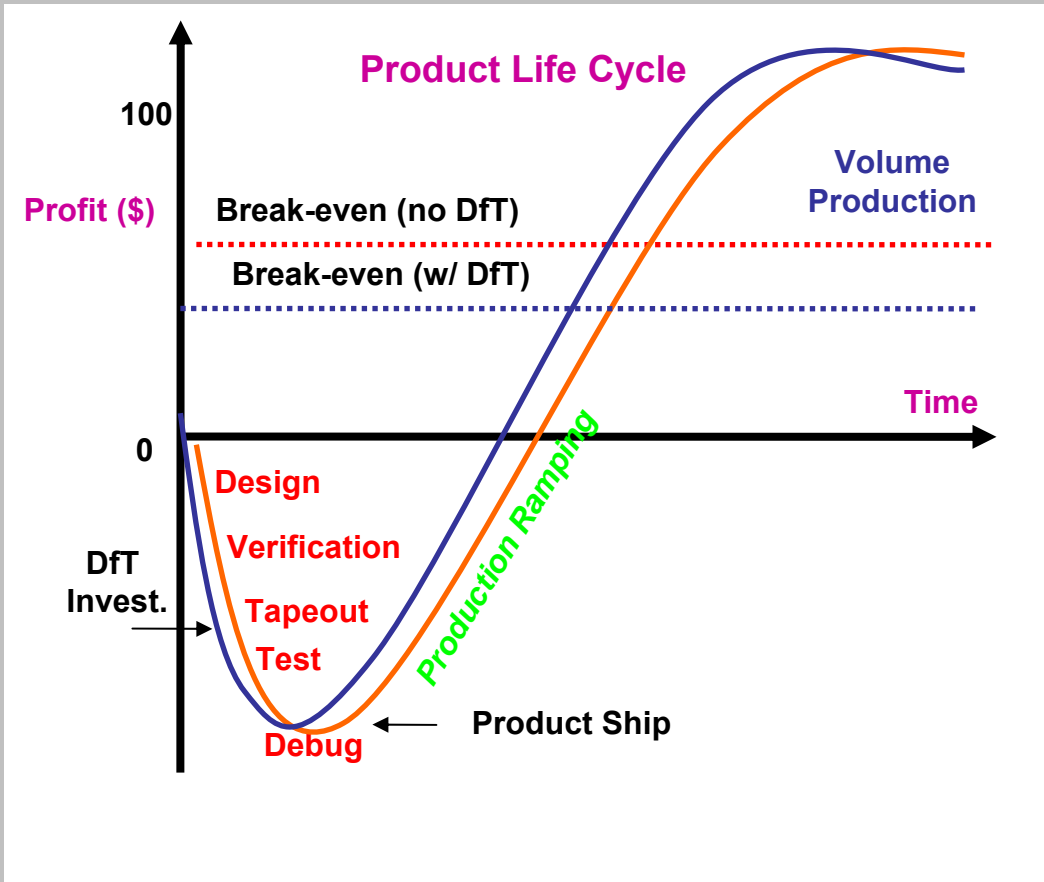
Agenda

- Introduction
- Motivation
- Proposed Built-in RF Testing Methodology
- RF Test Compaction Strategies
- Novel Spectrum analyzer-based sensor design
- Conclusions
- Future Work

Semiconductor Test and Reliability (STaRS) Laboratory – Current Projects

- DfT/BiST techniques for RF/AMS circuits (SRC)
- Low-power/high-performance digital/AMS circuit design
- Lifetest degradation and electronic characterization of SOAs (Corning, Inc.)
- Failure mechanisms and lifetesting of III-V material systems (MURI)
- Ballistic electronics (NSF)

The Business of Test



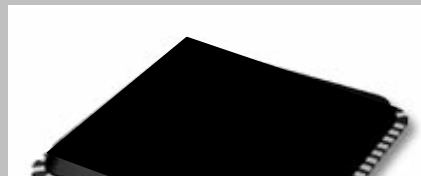
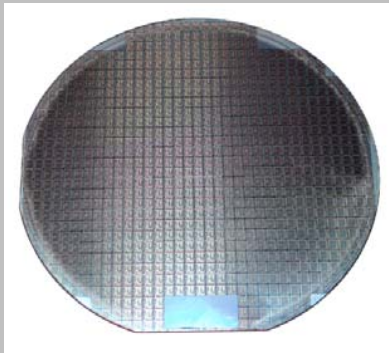
- Time-to-market drives profits
 - Faster return from investments
 - Competitive advantage
- Improving yield is KEY!
- DfT for RFIC production testing is limited
- FT (Functional Testing) is norm in industry
 - Most expensive investment (multi-million \$ ATE, highest test times)
- Test flow must accelerate time-to-market *efficiently*

AMS/RF IC Test Flow

WAT

(Beta, V_{th} , I_{OFF} , I_{ON})

Performed by
foundry



Wafer Probe
(I_{DDQ})

Performed by IC designer

Package Test
(Functional)

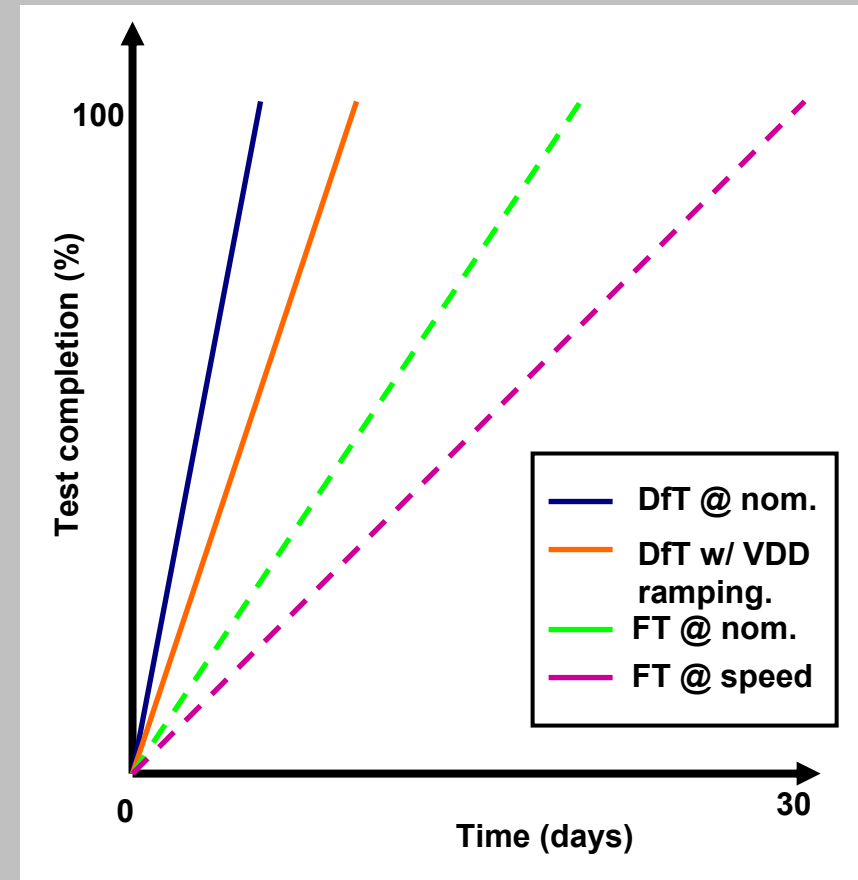


Cost
increasing
[\$]

Can we leverage Wafer Probe or WAT data to improve yield and reduce aggregate test costs?

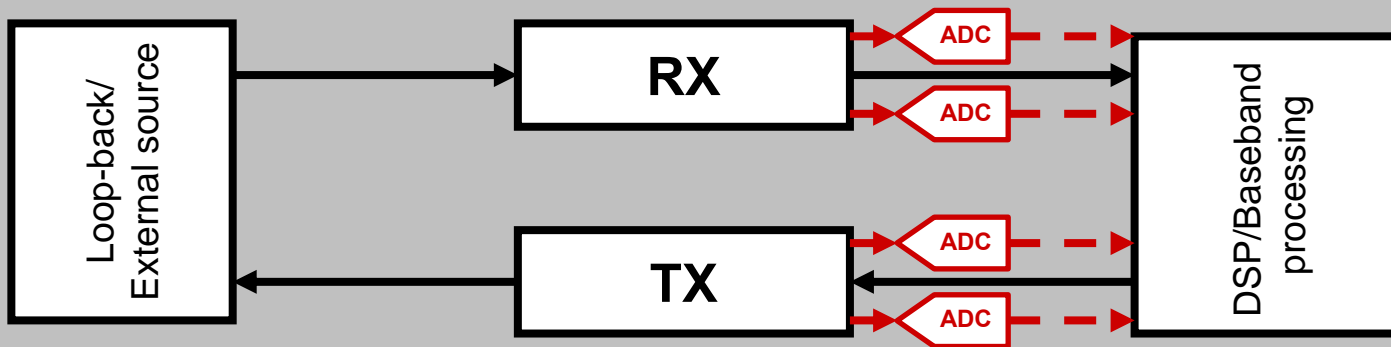
Built-in Test (BIT)

- Incorporate test circuitry directly on-chip (BIT)
 - Push ATE functions directly onto die
 - Cost of one TX is $<1 \mu\text{cents}$ for $0.25\mu\text{m CMOS}$ ¹
- BIT methodology must be more robust than device-under-test (DUT)
 - Subject to same PVT variation as DUT
- Power/Area overhead must be small
- **ADVANTAGES:** 1) Faster testing times 2) Higher observability
- Requires integration into design flow
- Difficult to maintain test quality metric
 - Test accuracy
 - Classification level
- Well-designed DfT will give high test coverage



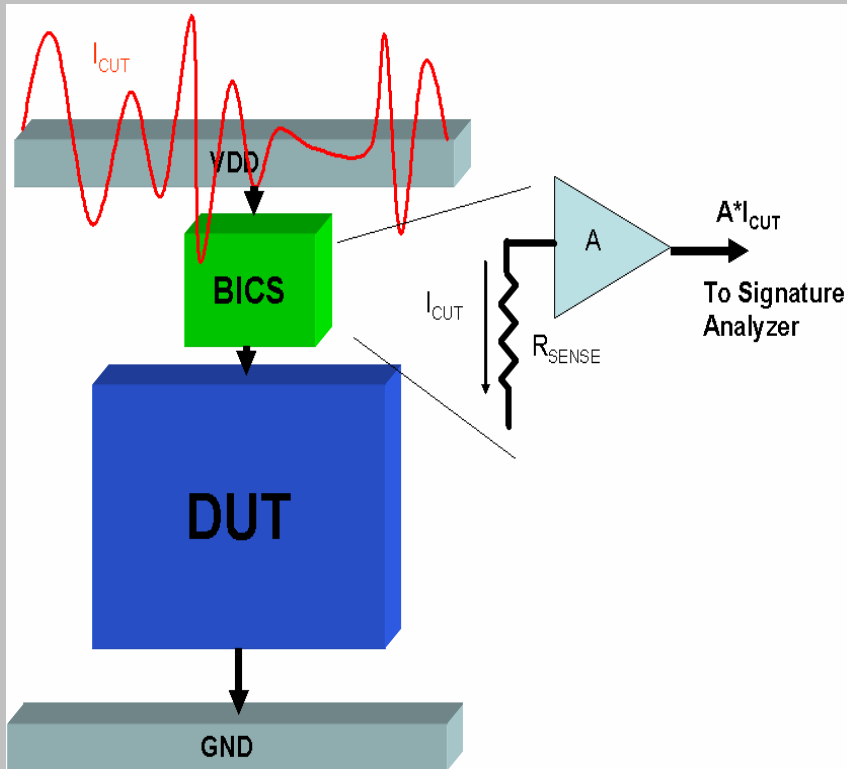
¹Adapted from W. Maly's "Cost of Silicon Viewed from a VLSI Design Perspective"

Classical Built-in RF Test Approach



- Reuse of already embedded components
- Sample test response utilizing embedded ADCs
 - GHz to multi-GHz sampling required
 - High-performance ADCs area/power hungry; low resolution
 - Sub-sampling possible; however, frequency response of ADCs limited to 500 MHz
 - Accuracy severely limited by jitter and PVT variations
- Include mixers to down-convert to low-IF frequencies
 - Additional overhead: area, power, phase alignment, etc...
 - Additional loss of accuracy

I_{DDQ}/I_{DDT} BIT

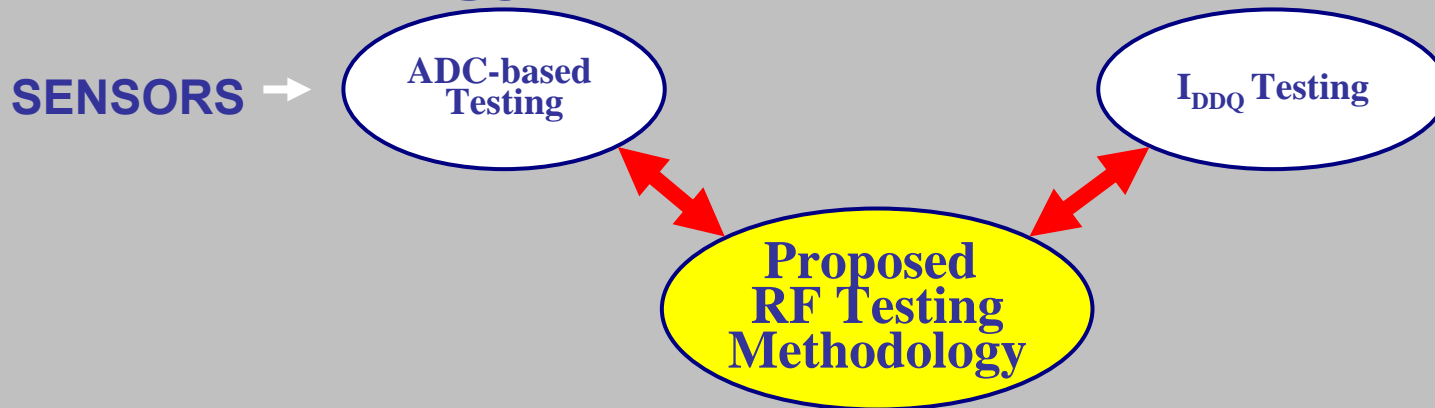


- Has been successfully utilized for about 25 years¹
- Utilizes DC or low-speed stimulus
- Fault detection by monitoring I_{DDQ} current
 - Structural (defect-oriented testing)
 - Faults cause fluctuations in quiescent (and transient) value
- Requires *Built-in Current Sensor* (BICS)
 - Prevalent in digital domain
 - Only handful of RF-suitable designs²

¹Levi, W., "CMOS is most testable," *IEEE International Test Conference*, Oct. 1981, pp. 217 – 220.

²Goplan, A., Margala, M., and Mukund, P.R., "A current based self-test methodology for RF front-end circuits," *Microelectronics Journal*, vol. 36, August 2005, pp. 1091 – 1102.

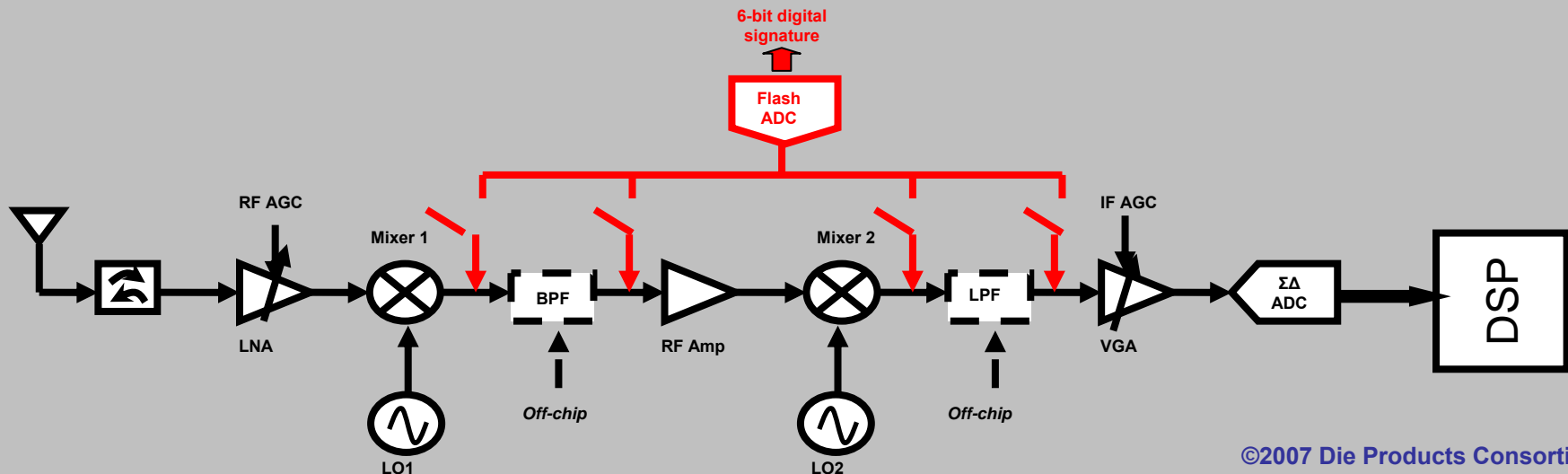
Proposed Built-in, Sensor-based RF Test Methodology



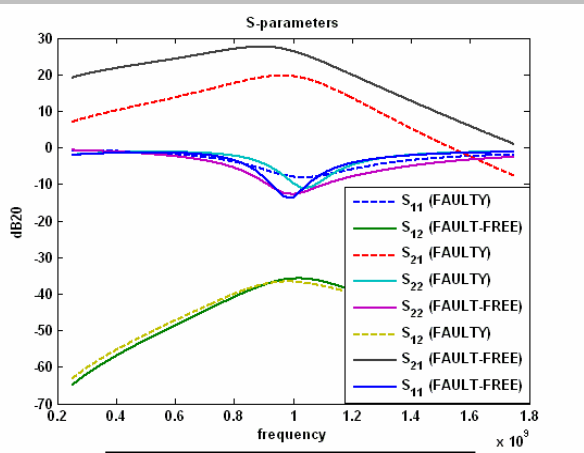
- Utilize signatures from embedded ADC and BICs to characterize RF DUT
 - GO/NO-GO testing scheme
- Structural-based approach rather than specification-based
 - Map **easy-to-measure** parameter to underlying test metrics
- DUT S_{21} and *IDD* current are test metrics
- Can be performed both at Wafer Probe AND after packaging
- Beneficial if implemented early in product design cycle
 - Test cost reductions

Test Considerations

- DUT is excited by loop-back hardware
- Embed portion of ATE functionality
 - **6-bit Flash ADC** digitizes DUT output signal
- Reuse chip resources
 - Frequency synthesizer (PLL) provides sampling clock
- Performance of ADC and PLL verified (*calibrated*)
- Degradations in S_{21} (voltage gain) are captured
 - GO/NO-GO Testing
 - Compared to “golden” signature [111111 (000000)]
 - PASS?: Perform rigorous functional-based testing
- Sampling performed at Nyquist (**2 GSamples/s**)
 - Coherent sampling (Additional synchronization circuitry)
- Only low-cost, digital test required
- Observability of gained through RF switches and active baluns

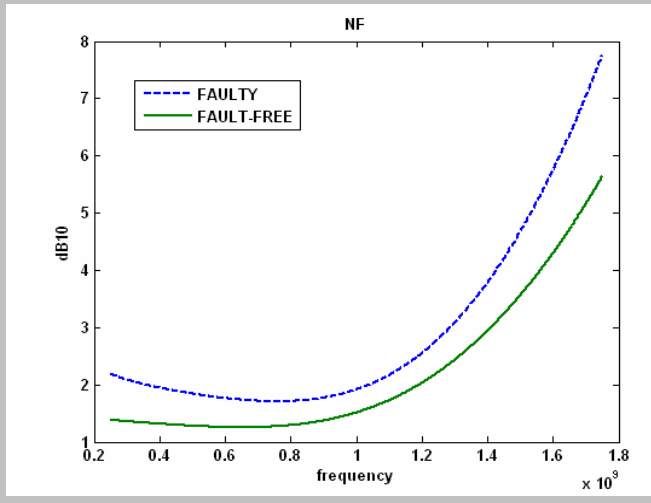


Simple Test Compaction

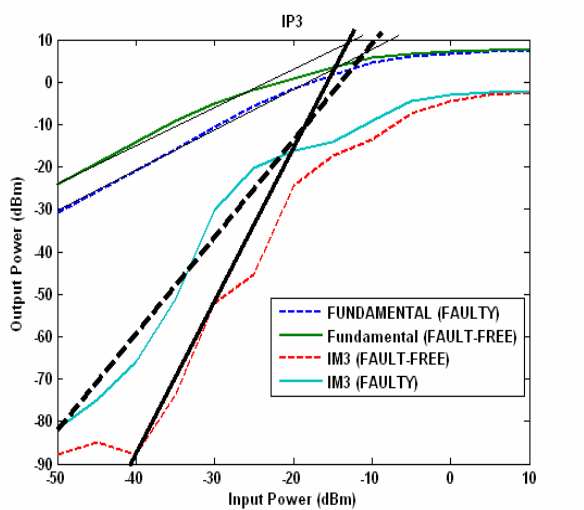


$$A_{IP3} = \frac{2}{\sqrt{3}} \left(\left| \frac{K_1}{K_3} \right| \right)^{1/2}$$

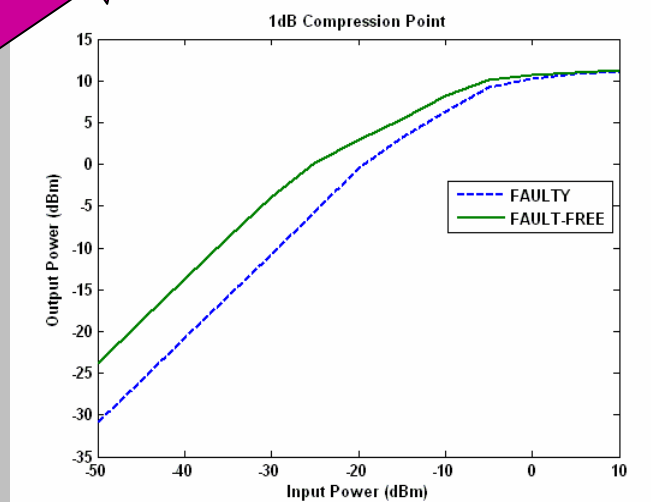
- Injection of faults cause modifications in all DUT RF performance parameters
- Performance degradation of RF DUT is highly correlated to S₂₁
 - NF, IIP3, 1dB compression point, ...
 - S₂₁ deviations can be theoretically related to presence of faults



$$NF = \frac{P_{NO}}{P_{Ni} * G_A}$$



$$G_A = \frac{P_{avn}}{P_{avs}} = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{|1 - S_{11} \Gamma_{in}|^2 (1 - |\Gamma_{OUT}|^2)}$$



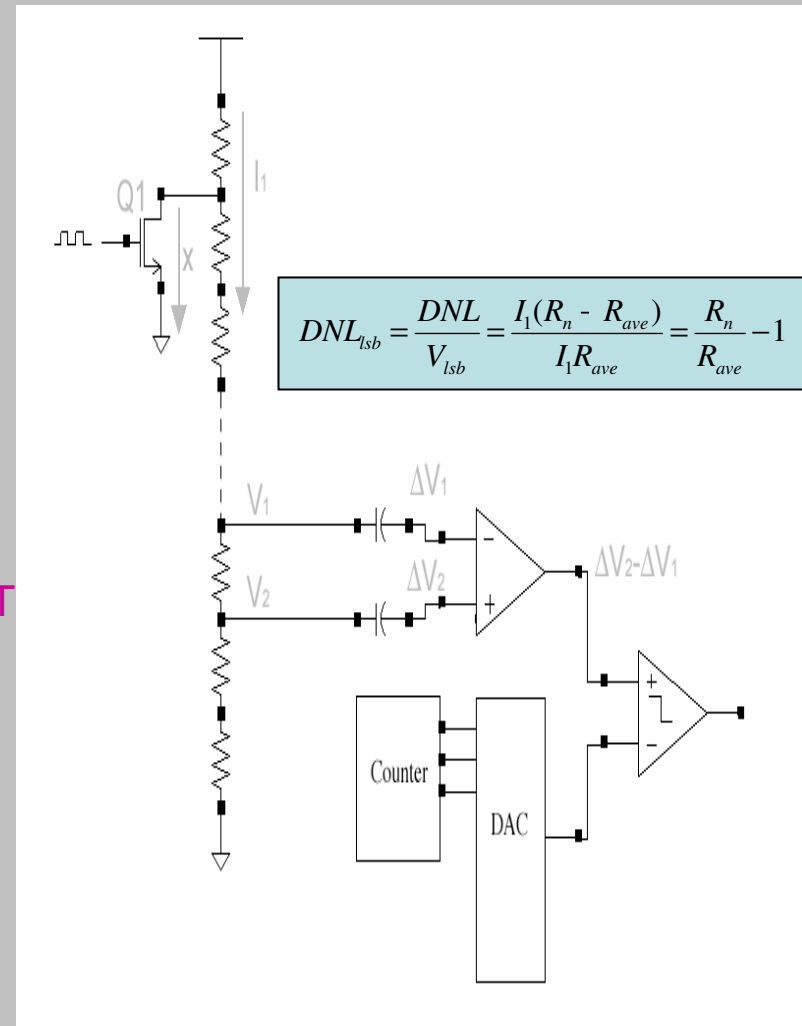
Summary of Fault Coverage Analysis

- 4 LNA architectures, 1 mixer architecture (folded-cascode), and 2 VCO topologies (ring and LC-tank) investigated
- **FAULT MODEL:** *Hard* (Catastrophic) -> Resistive Shorts; *Soft* -> Parametric
 - Fault model lacking
- **Differential and cascode LNA** and **both VCO designs** are the most sensitive to catastrophic faults
 - Fewest % of undetectable faults
- **Modified cascode LNA** and **mixer** are the least sensitive to catastrophic faults
 - Smallest gain parameter
- Most undetectable faults in **Reuse LNA** and **mixer**
 - Hidden in bias circuitry
- Fault masking prevalent in VCOs
 - Many fault locations shift/reduce tuning range
 - Faults can only be debunked if frequency of operation outside tuning range
- Ideal test configuration (highest sensitivity):
 - DUT: High S_{21} ; $S_{11} \sim -9$ to -10 dB
 - ADC: smallest full-scale range
- **Worst-case fault coverage of 89%**
 - Additional methods are necessary
 - Multiple fault insertion not considered

DUT	Largest Catastrophic Fault Detected [Sensitivity] (Ω)	Most Sensitive Parametric Parameter	Number of Undetected Faults (Number / % of Total)
LNAs			
Cascode	100k	V_{th} , L_{ind} , C_{MIM}	1 / 11%
Modified cascode	10k	V_{th} , L_{ind}	1 / 11%
Reuse	50k	V_{th} , C_{MIM} , R_{nwell}	3 / 11%
Differential	80k	V_{th}	1 / 4.8%
Mixer			
Folded cascode	40k	V_{th} , C_{MIM} , R_{nwell}	3 / 7.1%
VCOs			
Current-starved ring	10M	-	2 / 3.33%
Delay line-based differential	100M	-	5 / 6.67%

ADC BiST

- Verifies static performance of Flash ADC
- Q1 periodically draws a current (x) out of the steady-state current (I_1) of the resistive ladder
 - AC solution (rather than DC-based)
 - DNL can be extracted from measured current
- Subtractor measures differences in voltages
 - Result is proportional to resistance times ($1/x$)
 - Compared to DAC value
 - Digital value of resistance is stored
 - Measured value independent of x (high PVT variation immunity)
- Each resistor value in the ladder (R_n) as well as the average value (R_e) can be stored
- Faster than histogram-based approaches
- CONS:
 - Finite resolution (DAC)
 - Throw-away rate
 - High overhead (however, significantly smaller than histogram method)



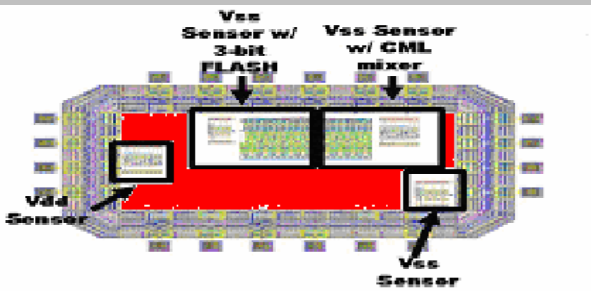
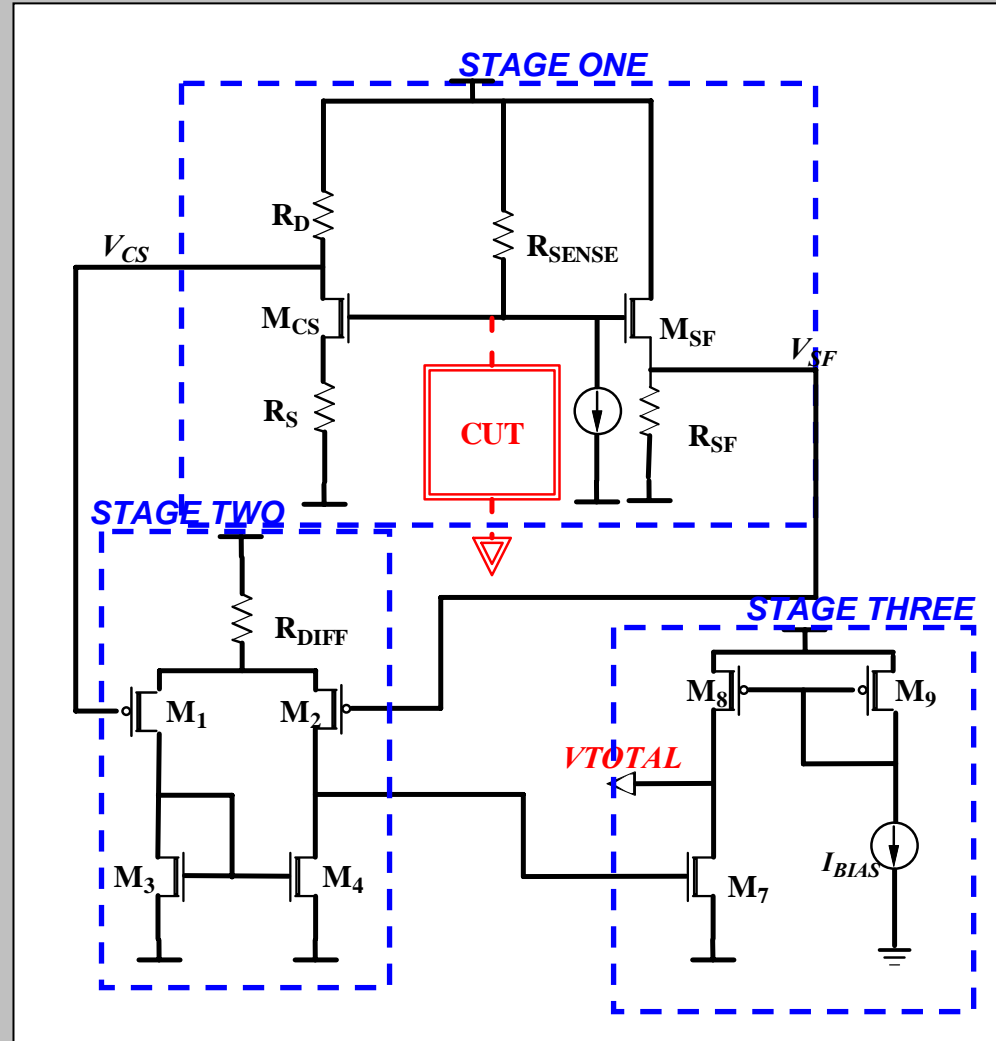
Challenges in Current-based Test for SOCs

Extremely stringent requirements on BICS:

1. Must be able to sense with high resolution large currents
2. Must have a high GBW product to sufficiently amplify small, high-frequency transients
3. Must be non-intrusive
4. Impervious to PVT variations

BICS Design

- Developed suite of BICSs based on same design
 - Low-bandwidth
 - High-bandwidth
 - Extremely temperature tolerant
 - Self-calibrating
- 3 Stage Design:
 - Stage One
 - Designed so that MCS and MSF are near their respective ZTC bias points
 - Current is sensed across 40 Ohm resistor
 - I - V conversion
 - Provides differential signals
 - DC current source prevents the sensor from saturating
 - Stage Two
 - Amplification stage
 - Stage Three
 - Final amplification
 - External bias for post-fabrication calibration
- V_{SS} BICS design includes additional DC level shifting stage



Monte Carlo Analysis

$m_u = 743.22 \text{ mV}$
 $\sigma = 17.2 \text{ mV}$

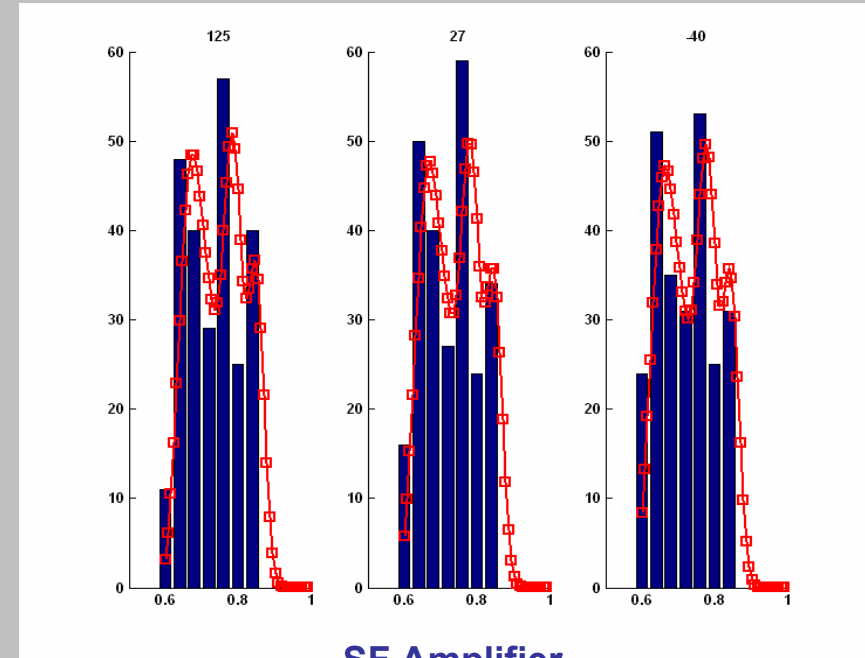
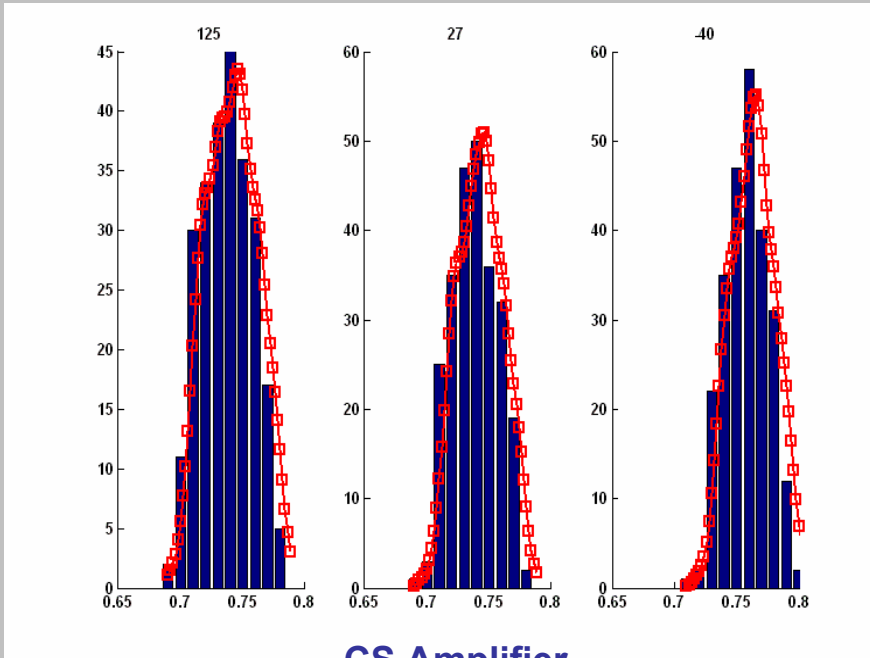
$m_u = 743.175 \text{ mV}$
 $\sigma = 17.96 \text{ mV}$

$m_u = 741.547 \text{ mV}$
 $\sigma = 20.16 \text{ mV}$

$m_u = 748.08 \text{ mV}$
 $\sigma = 71.26 \text{ mV}$

$m_u = 743.35 \text{ mV}$
 $\sigma = 72.57 \text{ mV}$

$m_u = 739.38 \text{ mV}$
 $\sigma = 73.3 \text{ mV}$



- 9 process parameters and V_{DD} varied with mismatch across the wireless operating temperature range [125°F to -40°F]
- DC output voltage of SF varies more with process variation
 - V_{SB} variance $\rightarrow V_{th}$ fluctuation
- DC output voltage of both amplifiers very stable with temperature

Performance Degradation Analysis

RF/analog benchmark cxts

Mixer Parameter	Normal Mode	Test Mode	Op-Amp Parameter	Normal Mode	Test Mode
Conversion Power Gain [dB]	4.89	4.82	DC Gain [dB]	33	32.2
Conversion Voltage Gain [dB]	1.89	1.82	3dB Freq. [MHz]	56.3	51.6
1dB Compression Point [dBm]	-1.894	-1.841	Unity Gain Freq. [MHz]	822	728
IIP3 [dBm]	10.1	11.2	PM [deg]	80	67
NF [dB]	4.57	4.71	Input Common-Mode Range [mV]	325	325
Power Consumption (3.3V Supply) [mA]	10	10	Output Swing [V]	1	1

Digital benchmark cxts

1000-Gate Logic	50 Gates Delay [ps]	100 Gate Delay [ps]	200 Gates Delay [ps]
@ I _{DDT1}	7.6	7.4	5.5
@ I _{DDT2}	8.38	10.56	13.71
@ I _{DDT3}	7.94	10.08	10.04
@ I _{DDT4}	8.39	10.74	12.77
@ I _{DDT5}	7.97	10.08	10.07
Average [ps]	8.06	9.92	10.42
2000-Gate Logic	50 Gates Delay [ps]	100 Gates Delay [ps]	200 Gates Delay [ps]
@ I _{DDT1}	4.48	5.38	4.98
@ I _{DDT2}	5.19	5.195	4.99
@ I _{DDT3}	9.73	9.38	9.82
@ I _{DDT4}	16.95	14.4	11.09
@ I _{DDT5}	23.4	20.3	21.35
Average [ps]	11.95	10.93	12.05

Comparison to other BICSs

	[57]	[55]	[52]	Proposed Design
Technology	0.35 μ m CMOS	BiCMOS	1.5 μ m CMOS	0.18 μ m CMOS
Sensing Device	FET Trans. (FTR)	Bipolar Trans. (BTR)	FET Trans. (FTR)	40 Ω Resistor (R)
# of Devices	65 FTR	2 BTR; 3 FTR	9 FTR	11 FTR; 4 R
3dB Bandwidth [MHz]	-	100	-	223.4
Area [mm ²]	0.08349	-	0.0097	0.0021
Clock signal	Yes	No	No	No
# of Control pins	4	0	2	2
# of Outputs	2	1	1	1
Temp. Stability	No	No	No	Yes
Process Stability	Yes	No	No	Yes

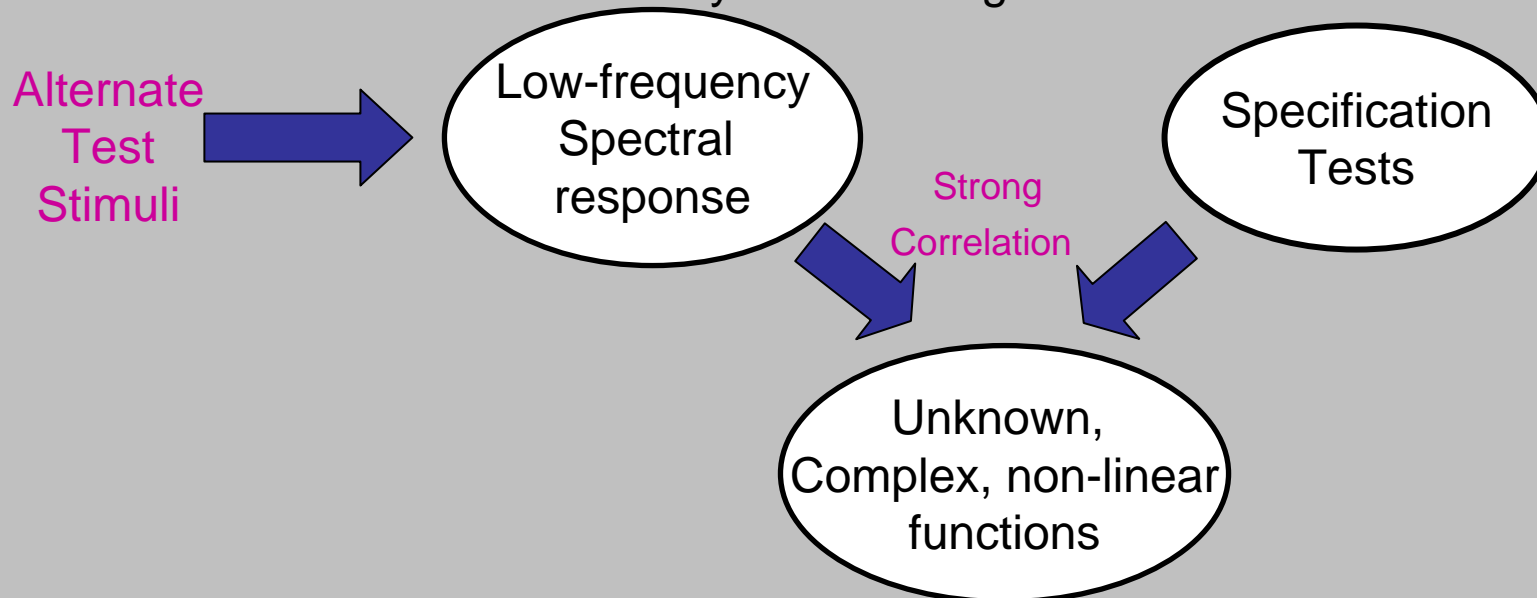
- Area discrepancy between [52] and proposed due to compensation cap for I_{DDT} testing
- Control pin overhead required
 - Most BICS designs require some calibration
- First design to show **BOTH** process and temperature tolerance

Agenda

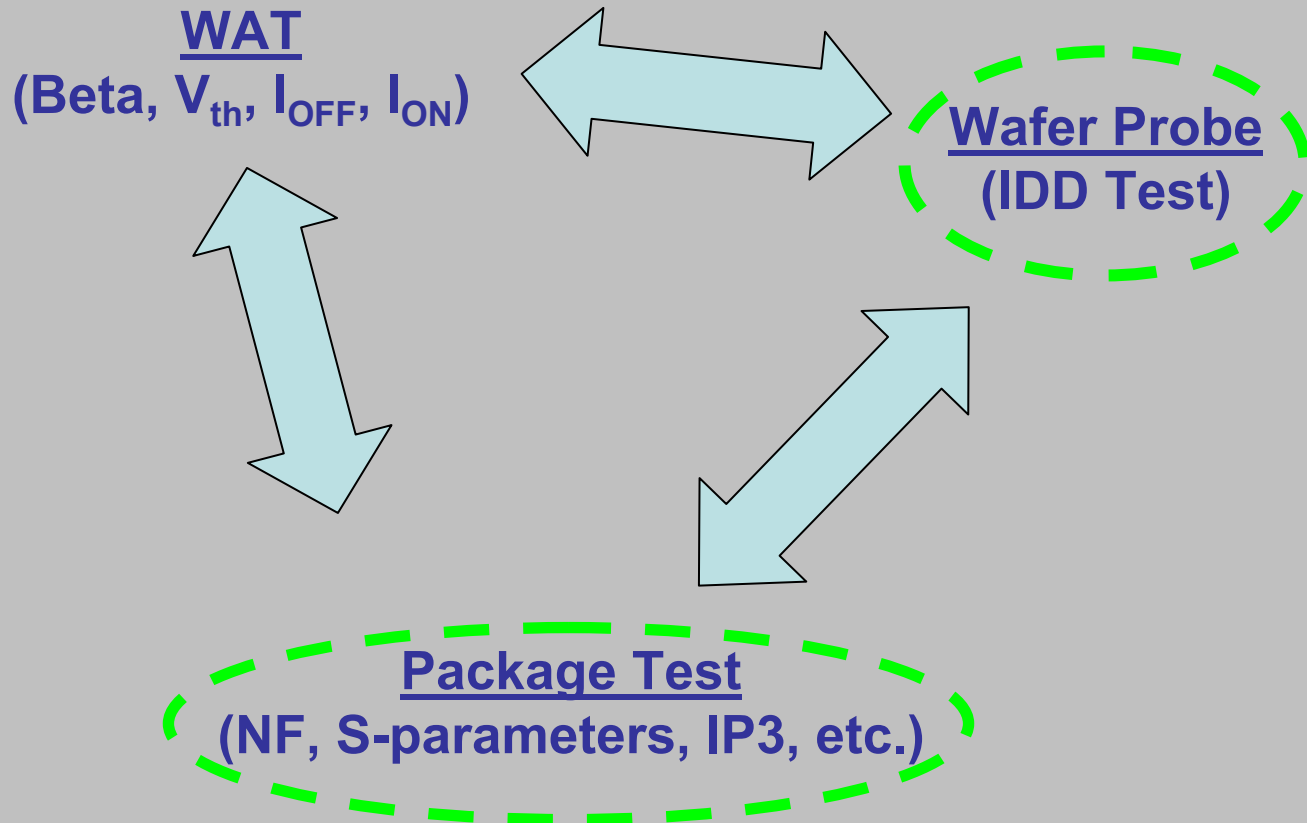
- Introduction
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- **RF Test Compaction Strategies**
- Novel Spectrum analyzer-based sensor design
- Conclusions
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Alternative Test Approaches

- Develop relationship between specifications and DUT response to some low-frequency/DC stimulus
 - High correlation between test response and specifications
 - Prediction of specifications from test response
 - Significant cost reductions possible
- *Regression vs. Classification?*
 - Tradeoff between accuracy and 'training' time

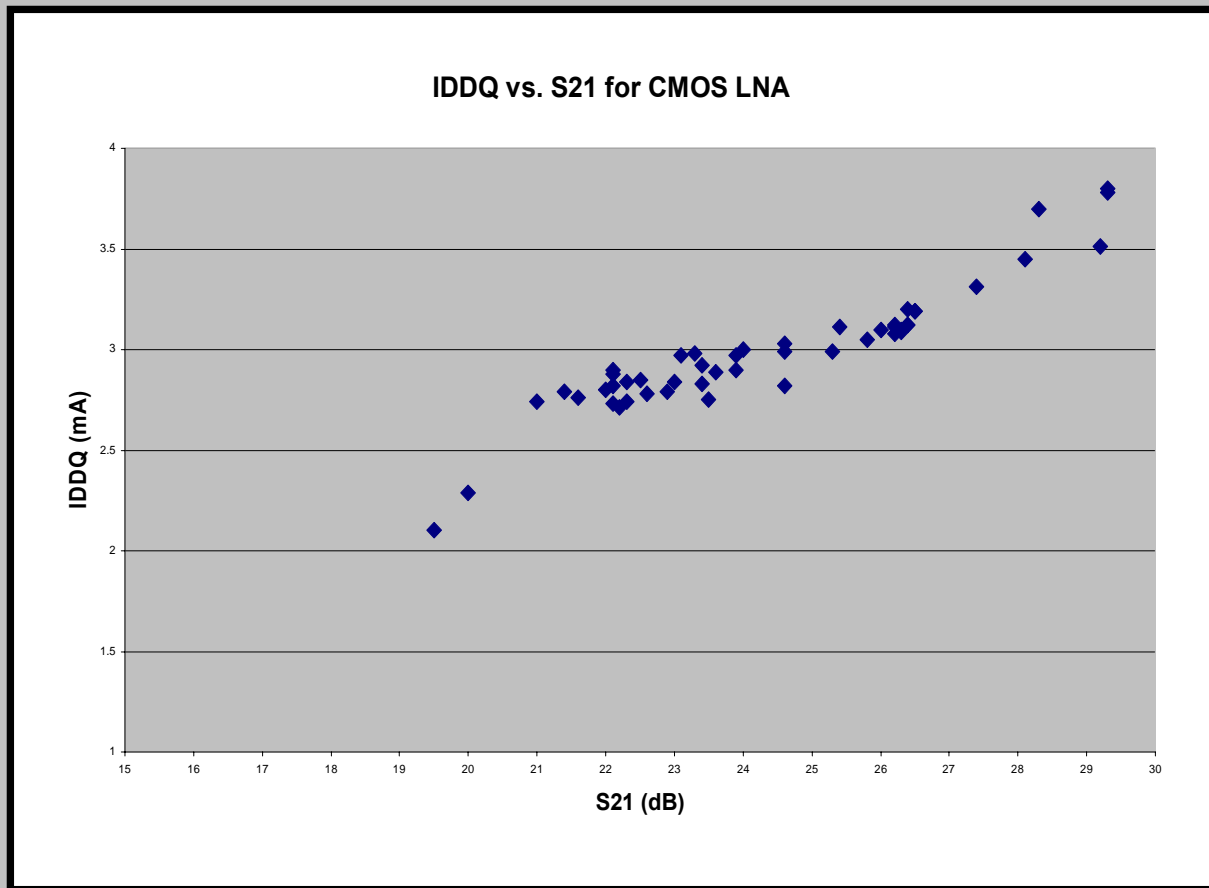


Test Compaction Strategy



GOAL: Develop highly correlated relationship between WAT, wafer probe, and package test

Preliminary Results



- 92% yield possible from using IDDQ data alone!

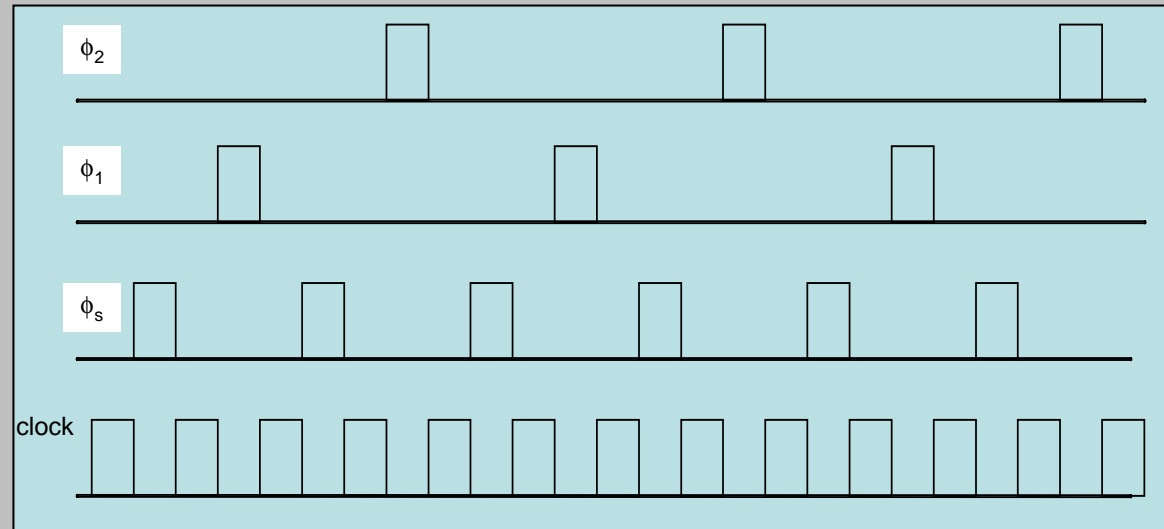
Is I_{DDQ}/I_{DDT} (Electrical Test) Enough?

- Results highly dependent on DUT, technology, test partitioning (accessibility), and BICS performance
- BICSs require some external calibration
- BICSs degrade performance of DUT
- *100% coverage most likely not achievable*

'Spectrum-analyzer' Sensor

- Spectral information will be necessary
- FFT Is computationally intensive
- Instead -> Utilize quantized sine and cosine basis functions
 - Similar to Walsh (Hadamard) codes
 - Basis functions can be stored in embedded memory
- Switched-capacitor implementation

$$X_{H_k} = \sum_{n=0}^{N-1} x[n] \cdot H_k[n]$$



In Summary

- Simple test compaction utilizing ADC-based RF test solution
 - PT-tolerant Flash ADC design
 - High confidence level in data signatures
 - Reduction in test cost early in design cycles
- Developed unique low-cost BiST solutions for Flash ADCs and CP-PLLs
- First PVT-stable BICS for digital/AMS/RF testing applications
 - Showed high correlation between BICS data and S_{21} for CMOS LNA
- Proposed simple switched-cap-based spectrum analyzer to extract additional information

Future Work

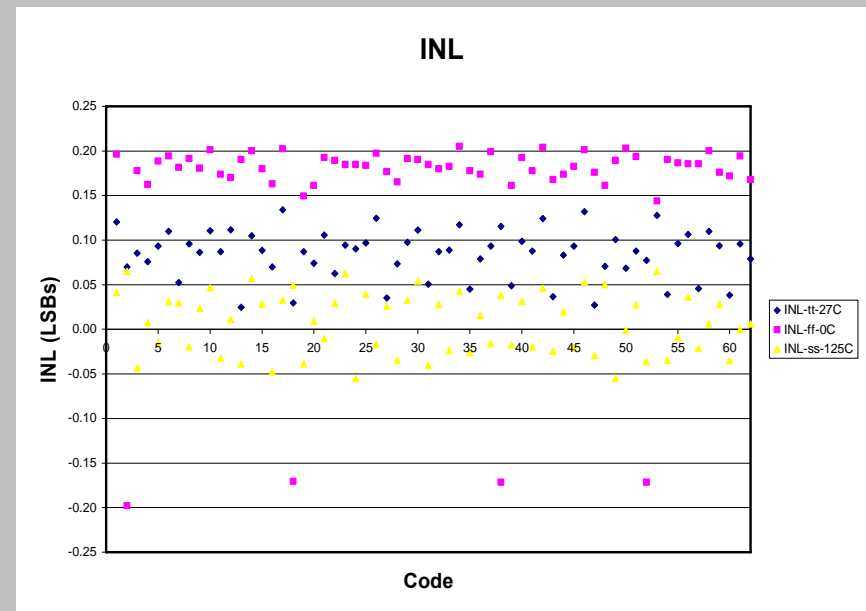
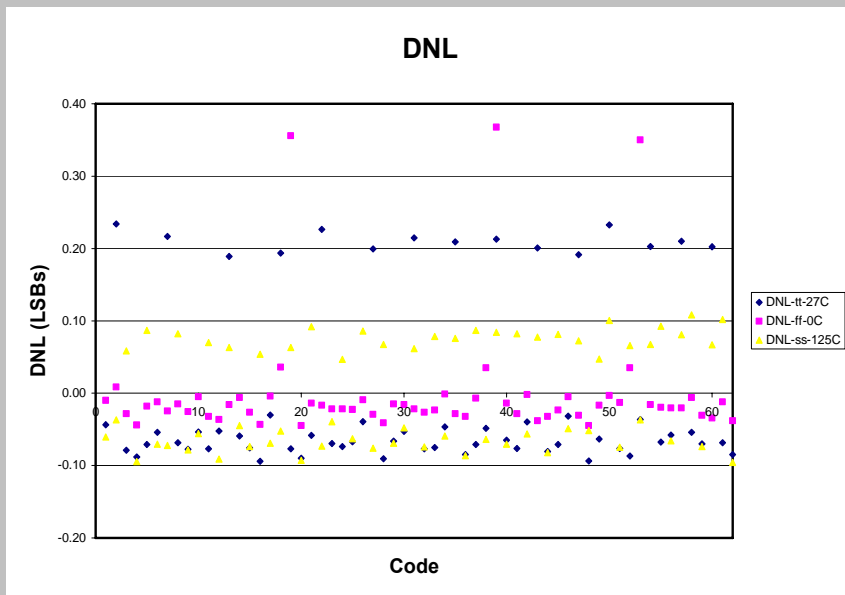
- Develop test bench and sensors resulting in high correlation between wafer probe and specification-based testing
 - Alternative-based testing approach
- Develop suite of low-overhead sensors suitable for characterizing digital/AMS/RF circuits
 - **Self-calibration** → **No external trimming required**
 - **Extract not only IDD current information, but other data useful to characterize DUT (temperature, process)**
 - **Post-process sensor data without utilizing power-hungry DSP**
→ **non-intrusive switched-capacitor-based spectrum analyzer**
- Develop ubiquitous fault model suitable for AMS and RF circuit applications
 - **Create tool suitable for integration into Cadence DFII environment that inserts various fault models (resistive, GOS, parametric, stuck-at, etc...) into spice netlist for degradation simulations**
- Self-calibrating AMS circuits for extreme operating conditions

Additional Slides

Relevant Publications

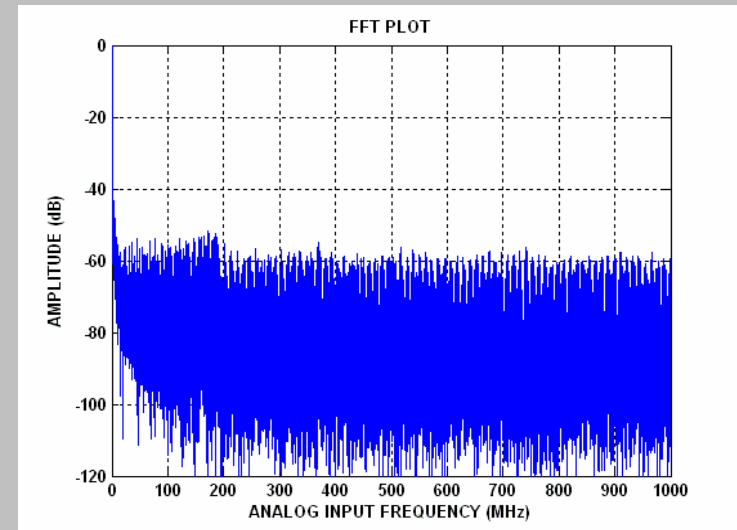
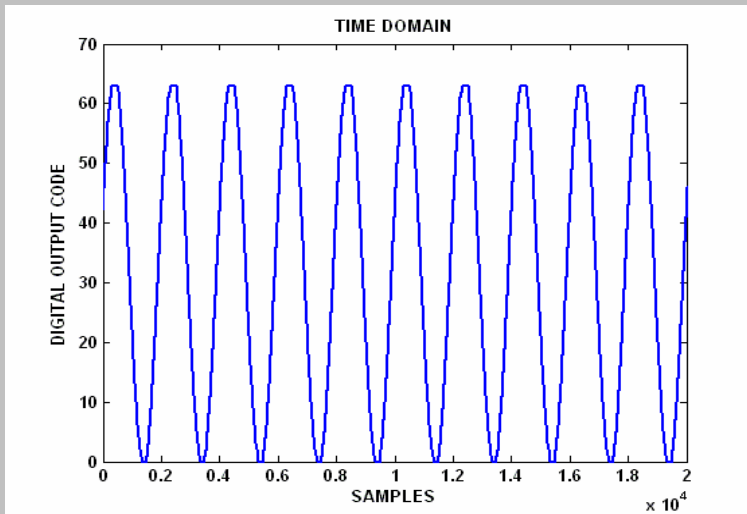
- [1] J. Liobe and M. Margala, "Novel Process and Temperature-Stable BICS for Embedded Analog and Mixed-signal Test," *IEEE Proceedings of IOLTS*, May 2007, pp. 231 – 236.
- [2] J. Liobe and M. Margala, "Novel Process and Temperature-stable, IDD Sensor for the BiST Design of Embedded Digital, Analog, and Mixed-Signal Circuits," *IEEE TCAS-I (In Press)*, May 2007.
- [3] J. Liobe, R. Geisler, and M. Margala, "A Novel Application of FM-ADC towards the Self-Calibration of Phase-Locked Loops," *2nd Revision Submitted to IEEE TCAS-I*, April 2007.
- [4] J. Liobe, R. Geisler, and M. Margala, "Process and Temperature Calibration of PLLs with BiST Capabilities," *Proceedings of the IEEE ISCAS*, May 2007.
- [5] J. Liobe, Q. Diduck, S. Ali, and M. Margala, "Process Tolerant Calibration Circuit for PLL Applications with BIST," *Proceedings of the IEEE ISCAS*, May 2006, pp. 2477-2480.
- [6] K. A. Jenkins, W. Rhee, J. Liobe, and H. Ainspan, "Experimental Analysis of the Effect of Substrate Noise on PLL Performance," *Digest of the 2006 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, June 2006, pp. 54-57.
- [7] M. Wieckowski, J. Liobe, Q. Diduck and M. Margala, "A New Test Methodology for DNL Error in Flash ADCs," *IEEE Symposium on Defect and Fault Tolerance in VLSI Systems*, October 2005, pp. 582-590.
- [8] M.S. Dragic, J. Liobe, and M. Margala, "New Sensor-based BIST for Digital and Mixed-Signal Circuits," *Proceedings of the IEEE North Atlantic Test Workshop*, May 2005, pp. 23 -30.
- [9] J. Liobe, X. Yunan, and M. Margala, "Testing Methodology for CMOS RF LNAs," *Digest of the IEEE RFIC Symposium*, June 2005, pp. 653-656.

Static Performance of Flash ADC



- ADC performance verified at BOTH temperature and process extremes
- **MAX. DNL = 0.37 LSB | MAX. INL = 0.21 LSB**

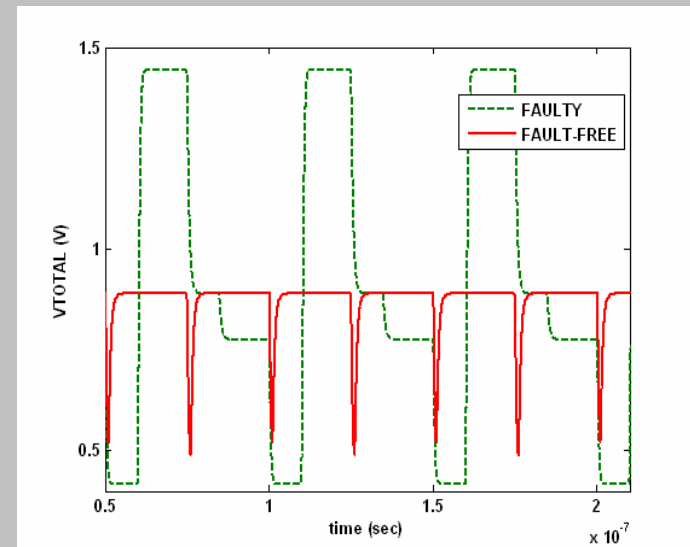
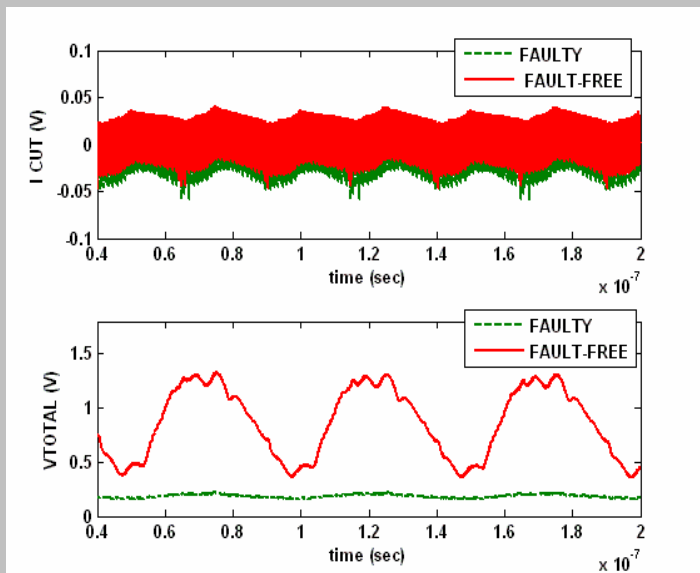
Dynamic Performance of Flash ADC



- Assuming noise due to clock jitter can be minimized (due to calibration), noise due to non-linearity (DNL/INL) dominates dynamic performance
- For chosen power constraint (< 50 mW), designed Flash ADC is only **5-bits** accurate (**SNDR = 31.983 dB**)
 - Error-correction techniques can be employed to re-attain last bit

BICS Catastrophic Fault Detection

- 10 kOhm D-S fault inserted in mixer
 - Significant change in mixer I_{DD} current waveform tracked by BICS
 - LO (high frequency) noise filtered by input stage and sensing resistor



- Resistive fault is inserted in one NAND gate in 500-gate sample
- For fault-free condition, DC output of BICS remains around 0.9 V
- However, for a 10 kOhm G-S fault:
 - $\Delta I_{DDQ} = 156\text{mV}$
 - $\Delta I_{DDT} = 465\text{mV}$
- High frequency transient also detected