



Testing the Limits
FOR PRODUCT SUCCESS

DRAM Die Thickness vs. Yield and Reliability Study



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AGENDA

- Motivation for study
- Methodology used
- Findings and Conclusions
- Summary
- Possible Solutions
- Inapac Solution
- Special Acknowledgement



Motivation For Study

- Strong need in stacked die applications
 - SiP/MCP height constraints in cellular handsets
 - Trend is more dice, thinner dice (Application processors, Media processors, Image processors, Basebands)
- Request by sophisticated customers
 - Require DRAM dice as thin as 80um
 - Understand that die thinning has a large process dependency, ie. each process can have a potentially different result at the same die thickness
 - Want to understand yield and reliability implications
- No public domain data is available on impact to DRAM die due to thinning



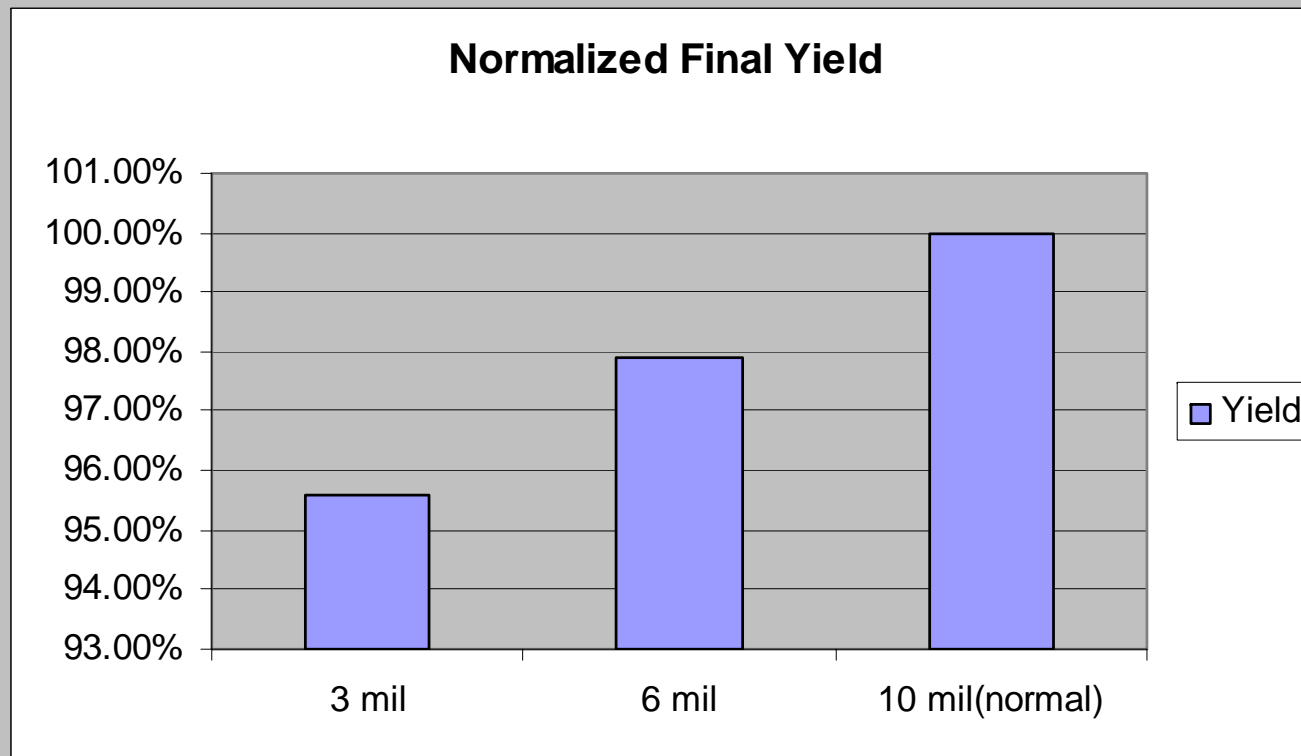
Methodology

- One wafer lot (25 wafers) was pulled from production line for this study (sample size >14,000)
 - 512Mbit, DDR2 commodity DRAM (300mm)
- These 25 wafers were divided into 3 assembly lots
 - Wafer 17-25 (10mil/250um) -- standard flow
 - Wafer 9-16 (6mil/150um)
 - Wafer 1-8 (3mil/75um)
- After assembly is completed, all 3 lots follow standard commodity DRAM production flow.
 - BI-> FT3 (-10C)->BT2 (90C)
- Only controlled variable is die thickness



Result Summary (Normalized Data)

- Data shows over all yield* degradations as DRAM dice become thinner

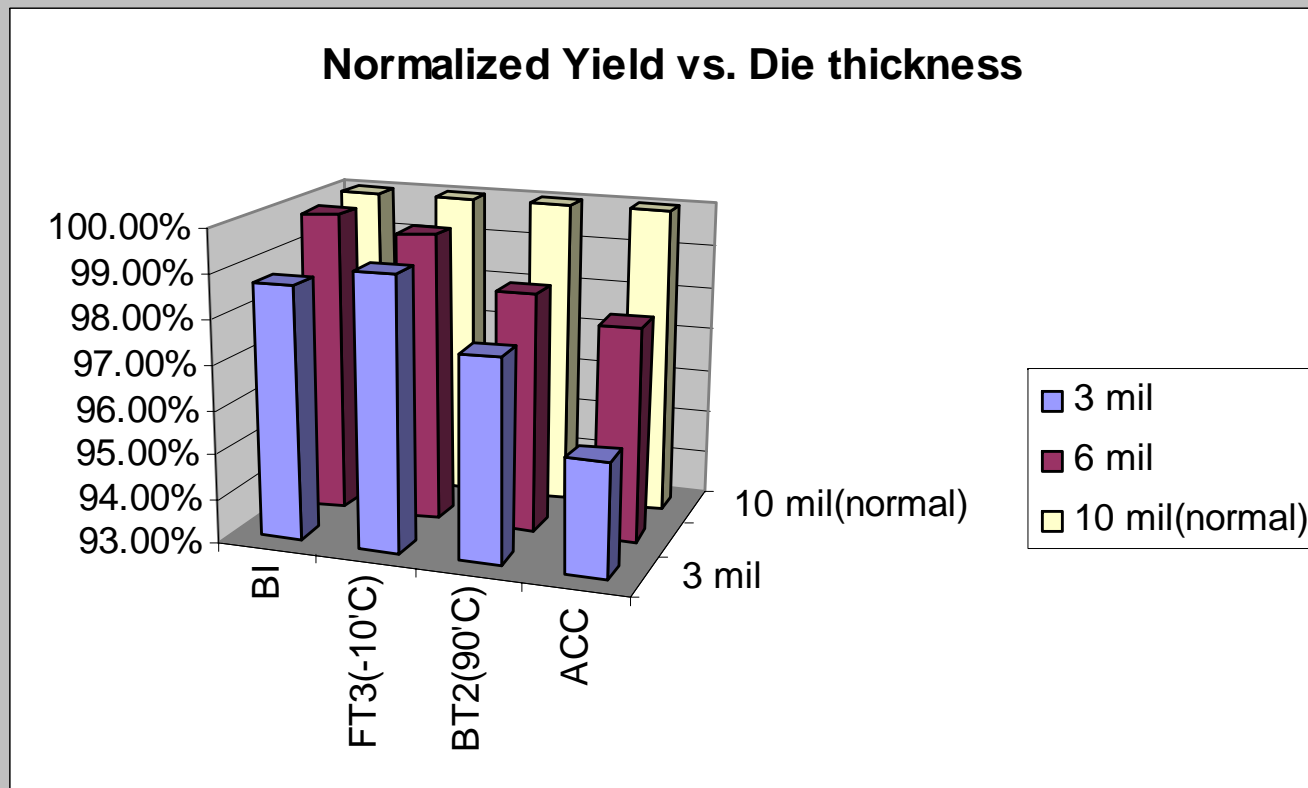


* Yield normalized to 10mil. Inapac customers and partners under NDA have access to raw data.



Result Summary (Normalized), Cont.

Backend Yield cor	BI	FT3(-10'C)	BT2(90'C)	ACC
3 mil	98.77%	99.17%	97.60%	95.59%
6 mil	99.87%	99.57%	98.43%	97.88%
10 mil(normal)	100.00%	100.00%	100.00%	100.00%

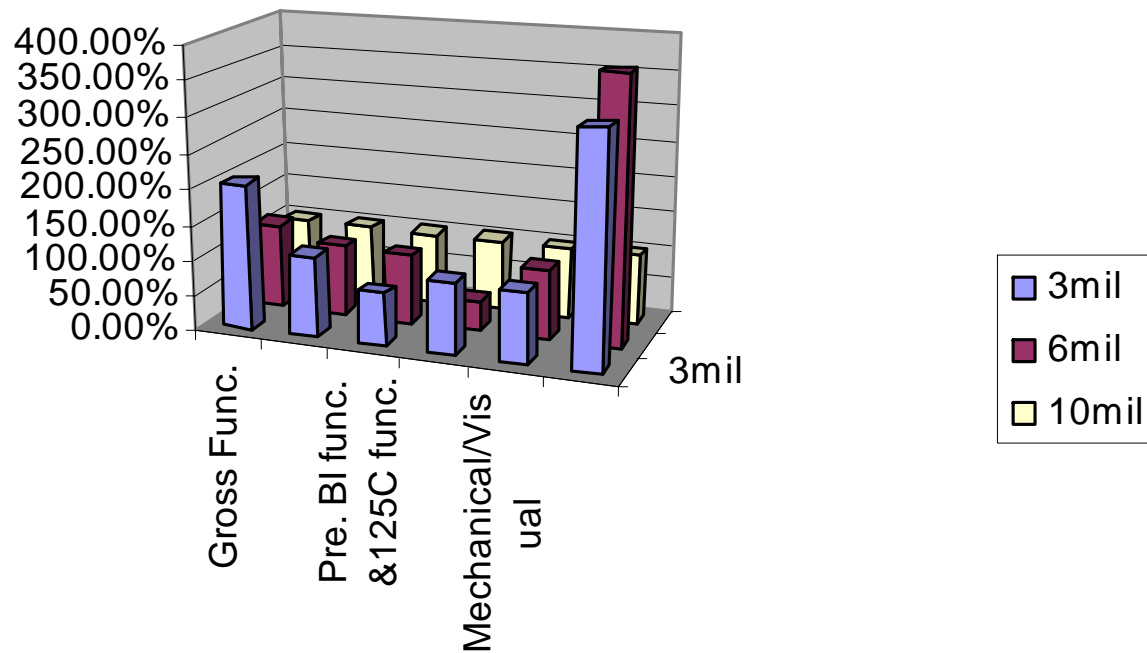




Smart Burn In Pareto (Normalized)

Normalized BI Pareto	Gross Func	Other Func.	Pre. BI func. & 12	Chipping	Mechanical	Pre-test fail
3mil	206.38%	113.51%	74.47%	100.00%	100%	325.00%
6mil	121.28%	101.21%	97.87%	42.31%	100%	375.00%
10mil	100.00%	100.00%	100.00%	100.00%	100%	100.00%

Normalized BI Pareto



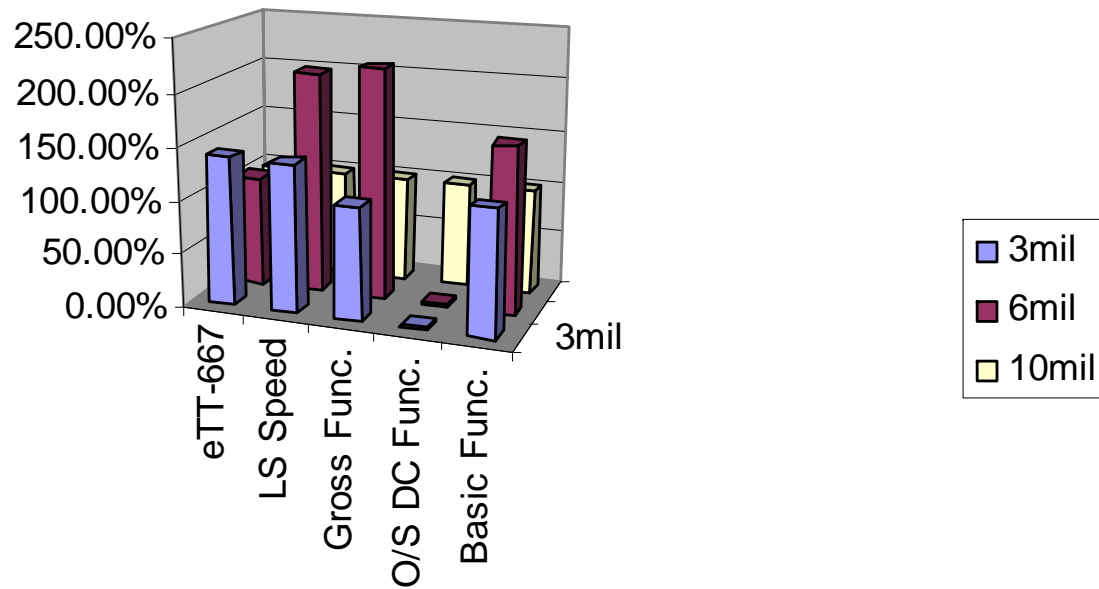


FT3 (-10C) Pareto (Normalized)

Normalized FT3 Pareto	eTT-667	LS Speed	Gross Func.	O/S DC Func.	Basic Func.
3mil	141.11%	140%	106.25%	2.63%	118.63%
6mil	105.23%	210.00%	218.75%	2.63%	157.84%
10mil	100.00%	100.00%	100.00%	100.00%	100.00%

Note: Bad DUT.

Normalized FT3 (-10C) Pareto

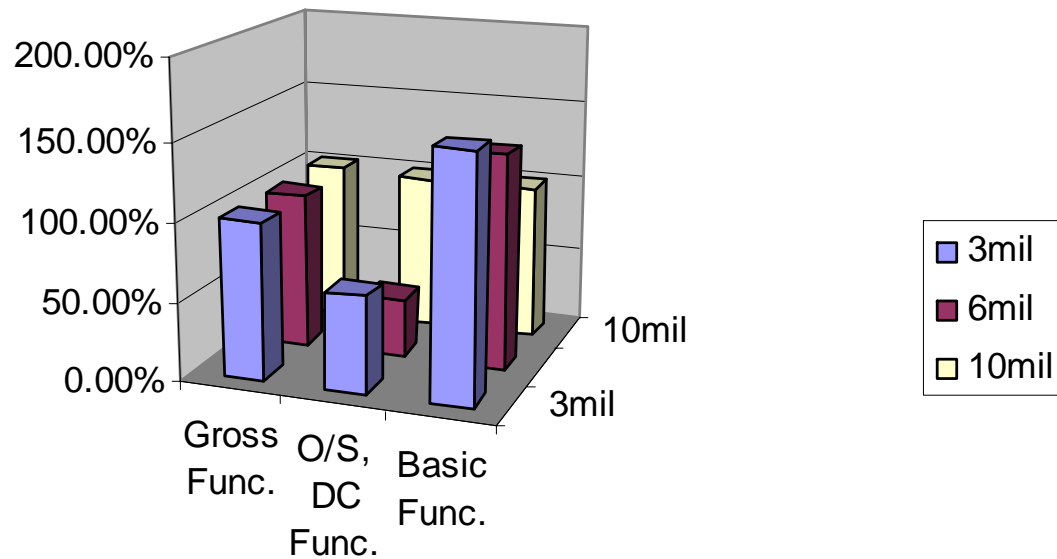




FT2 (90C) Pareto (Normalized)

Normalized FT2(90C) Pareto	Gross Func.	O/S, DC Func.	Basic Func.
3mil	100.00%	61.54%	155.24%
6mil	100.00%	38.46%	137.53%
10mil	102.00%	100.00%	100.00%

Normalized FT2 (90C) Pareto

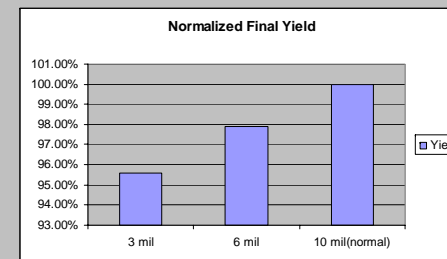




Conclusion:

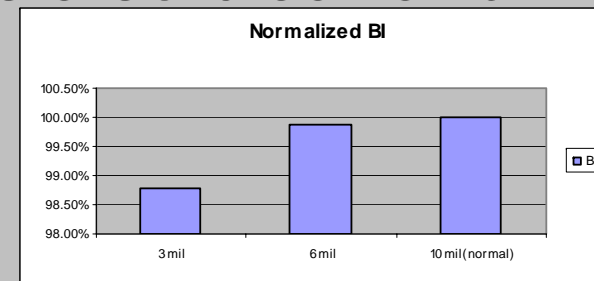
- Study shows a clear and linear correlation between DRAM die thickness and final over all yield.

- Thinner die, lower yield



- Reliability correlation (IM) is also clear and linear.

- Thinner die, lower BI yield



- *KGD may no longer be KGD after wafer thinning!*



Summary

- The study shows a significant impact to DRAM die due to thinning
- Ability to measure this impact in stacked die applications is crucial
 - A marginal bit can crash OS!
- A DFT based production methodology can help
 - Inapac's SiPFLOW platform
- Yield lost vs. test escape
 - Based on the data, ~4% yield was lost due to die thinning to 3 mil. We know this from $BI \cdot FT^3 \cdot BT^2$
 - Without BI and FT (as KGD is defined), the result of die thinning would translate into ~4% test escape in this case.



Solutions?

- How to detect BSG related KGD yield loss at 3 mil, if you can not reduce them ?
 - BSG before CP?
 - Can it be done at 3 mil?
 - Has it been done at 3 mil?
 - How costly is it?
 - Will assembly subcon. even try it?
 - BIST
 - Cost?
 - Test coverage?
 - Others?
- A practical solution is needed for high density/low profile packages using DRAM die(dice)!



Inapac's solution is more than KGD!

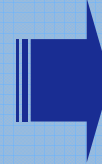
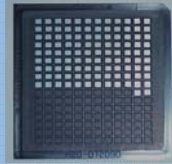
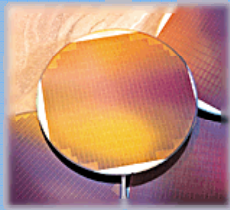
- A solution for Known Good Device
 - SiP/PoP/PiP/MCP/XYZ.....
- A DFT methodology to ensure that DRAM is reliable, regardless of the package type or die thickness
- We solve the problem that needs to be solved
 - A practical and low cost approach



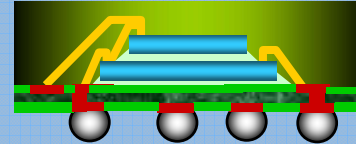
Inapac Solution:

SiPFLOW™ Methodology

DFT Enabled
Memory Device



SiP/MCP
(LOGIC + DRAM) or (Flash + DRAM)



Better quality
Better reliability
Memory die

High quality
High reliability
SiP/MCP

Wafer Level Tests

- VIBE™ Wafer Level Test
- Proprietary Screen Tests
- **No Wafer Level Burn-in**

Package Level Tests

- SiPLINK™ Test Access
- Full Access Final Test
- **No "Pin Tax" on Package**

Product
Lifecycle Cost
Optimization

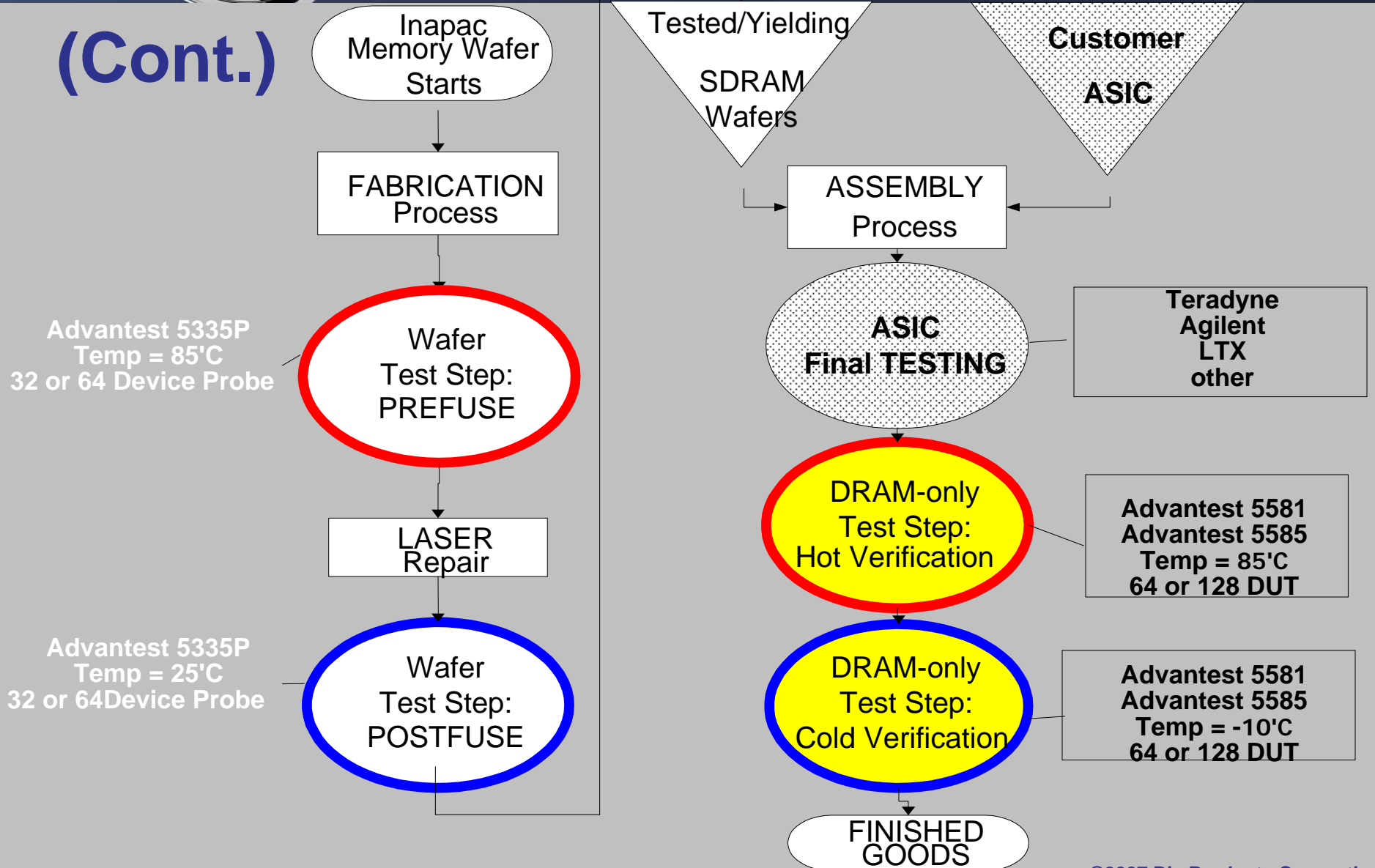
**Cost Effective Solution For Maximizing SiP/MCP
Yield and Reliability**

Testing the Limits

FOR PRODUCT SUCCESS



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- Full access FT capability detect die thinning issue during production
- Package level VIBE™ available to provide additional reliability screening/verification during production



Special Acknowledgements

Thank You!

ProMOS Technology and ChipMOS Technology for providing study materials, personnel and world class services. This study would not have been possible without their generous assistance