15th Annual KGD Packaging & Test Workshop

2008

AGENDA

Sunday, September 7, 2008	
5:00 pm – 7:00 pm	**Welcome Reception and Workshop Check-In**

Monday, September 8, 2008	
	Session 1: Special Topics Session Chairs: Georg Meyer-Berg, Infineon Technologies & Tetsuya Onishi, Grand Joint Technology
9:00 am – 10:00 am	9:00 **Keynote Presentation:** **Main Drivers of New Packaging Technology Research & Development** Mario Bolaños-Avila, Texas Instruments
10:00 am – 10:30 am	**Break, Exhibits Open**
10:30 am – 12:00 pm	10:30 **Saving Energy with Advanced Power Semiconductors** Dean Henderson, Infineon Technologies 11:15 **High Power LEDs for Solid State Lighting: Status, Trends, and Challenges** Bob Steward, Philips LumiLeds Lighting Company
12:00 pm – 1:30 pm	**Lunch Sponsored by Chip Supply and Texas Instruments (Atrium)**
	Session 2: Test Infrastructure Session Chairs: Lee Nevill, Micron & Jim Rates, Chip Supply, Inc.
1:30 pm – 3:00 pm	1:30 **Probing for Known Good Die** Rob Marcelis, Salland Engineering 2:00 **BGA/CSP, LGA/QFN Test Solutions & Interconnect Technology with SPIRAL CONTACT™** Scott Hirai, Advanced Systems Japan, Inc. 2:30 **Super Sockets - Integrating Technology - Test Board to Socket** Thomas Bresnan, R&D Circuits
3:00 pm – 3:30 pm	**Break, Exhibits**
3:30 pm – 5:00 pm	3:30 **Introduce Burn-in and Final Test Socket with Spiral Contact™ from Advanced Systems Japan Inc.** Shin Yoshida, ALPS Electric Co, LTD 4:00 **Wafer Level and KGD Test for Power Devices** Don Feuerstein, SemiProbe 4:30 **Fault Counting Standardization** Rohit Kapur, Synopsis, Inc.
5:00 pm – 7:00 pm	**Wine & Cheese Reception in Exhibits Area**

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Tuesday, September 9, 2008	
	Session 3: KGD Engineering Session Chairs: Jim Wolbert, Chip Supply, Inc. & Peng Lin, Qualcomm
9:00 am – 10:30 am	9:00 **Dry Polishing of Wide Band-gap Semiconductor Wafers** Scott Sullivan, Disco Hi-Tec America 9:30 **Enabling Technologies for Differentiated End Products** Dean Henderson, Infineon Technologies 10:00 **Ultra-Thin Chip Manufacturing for New Packages** Peter Heinze, PVA TePla AG
10:30 am – 11:00 am	**Break / Exhibits**
11:00 am – 12:00 pm	11:00 **When Known Good Die Go Bad: The Power of Failure Analysis** Tom Weldon, Micron 11:30 **Intelligent - not Total Recall** Dave Huntley, Kinesys Software
12:00 pm – 1:00 pm	**Lunch (Atrium)**
	Session 4: Test Methods Session Chairs: Ken Ball, Knowledge Based Tech Consultancy & Jeanne Beacham, Delphon Industries
1:00pm – 3:00 pm	1:00 **A New WBI DOE Methodology to Break Through High BurnIn Power Consumption in Nano & Giga Era** Gibum Koo, Samsung Electronics 1:30 **Semiconductor Test: From Back-End To Center Stage** Bill Price, Optimal Test 2:00 **Strategies for Low-cost Testing Above 10 Gbps** David Keezer, Georgia Institute of Technology 2:30 **Robustness Validation - A New Strategy for Automotive Semiconductor Quality** Peter Wilson, ON Semiconductor
3:00 pm – 3:30 pm	**Last Chance to Visit Exhibits**
3:45 pm	**Buses depart for Sebastiani (Meet in Embassy Suites lobby)**
4:00 pm – 6:00 pm	**Private Tour of Sebastiani Winery**

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Wednesday, September 10, 2008	
	Session 5: Advanced Packaging Session Chairs: Larry Gilg, Die Products Consortium & Georg Meyer-Berg, Infineon Technologies
9:00 am – 12:00 pm	9:00 **Overview of the FC and WLP market** Jan Vardaman, Techsearch International 9:30 **Requirements for Cost-Effective 3D Integration** Philip Pieters, IMEC 10:00 **Chip-Stacking for TSV** Kunio Yoshida, AJI Co. Ltd. 10:30 **Chip In Wafer for Integrated System** Jean-Charles Souriau, CEA-LETI Minatec 11:00 **KGDs and Embedded Substrates Join Hands to Drive Cost & Form-Factor in Mobile Applications** Arun Amirtham, NXP Semiconductors 11:30 **Die Products Embedded Component Trend** Tetsuya Onishi, Grand Joint Technology, Ltd.
12:00 pm	**End of Workshop, Boxed Lunches for Take-Away**