

Cost Comparison Between Sacrificial Metal Wafer Level Burn-in and Test (SM WLBT) vs. Package Burn-In and Test

**Walid Ballouli, 8/16 Bit Microcontroller Product Manager, Motorola (r14749@motorola.com)
6501 William Cannon Drive West, MD OE312; Austin, Texas 78735; 512-895-8639**

**Teresa McKenzie, Wafer Level Burn In Engineer, Motorola (T.McKenzie@motorola.com)
6501 William Cannon Drive West, MD OE311; Austin, Texas 78735; 512-895-4826**



Agenda / Outline

Burn-In Overview

Primary Attribute Differences

Package Burn-In Cost Attributes

Package Cost Analysis Equations

SM WLBT Cost Attributes

SM WLBT Cost Analysis Equations

SM WLBT Forecast vs. Actual Cost

Summary



KGD Sacrificial Metal WLBT

- Definitions -

- **Wafer Level Burn-In and Test (WLBT)**

Parallel, dynamic, excitation of all devices on a wafer to screen marginal devices for infant mortality by dynamically stressing the integrated circuit at elevated temperature and voltage. Capable of non-volatile memory cycling, module exercising, and testing.

- **Known Good Die (KGD)**

Die having the same quality and reliability level as that of an equivalent packaged part.

- **Sacrificial Metal (SM)**

Metal which is temporarily deposited on the wafer to provide electrical signal paths to a die during wafer level burn-in and test. The sacrificial metal is etched away after burn-in and test is complete.



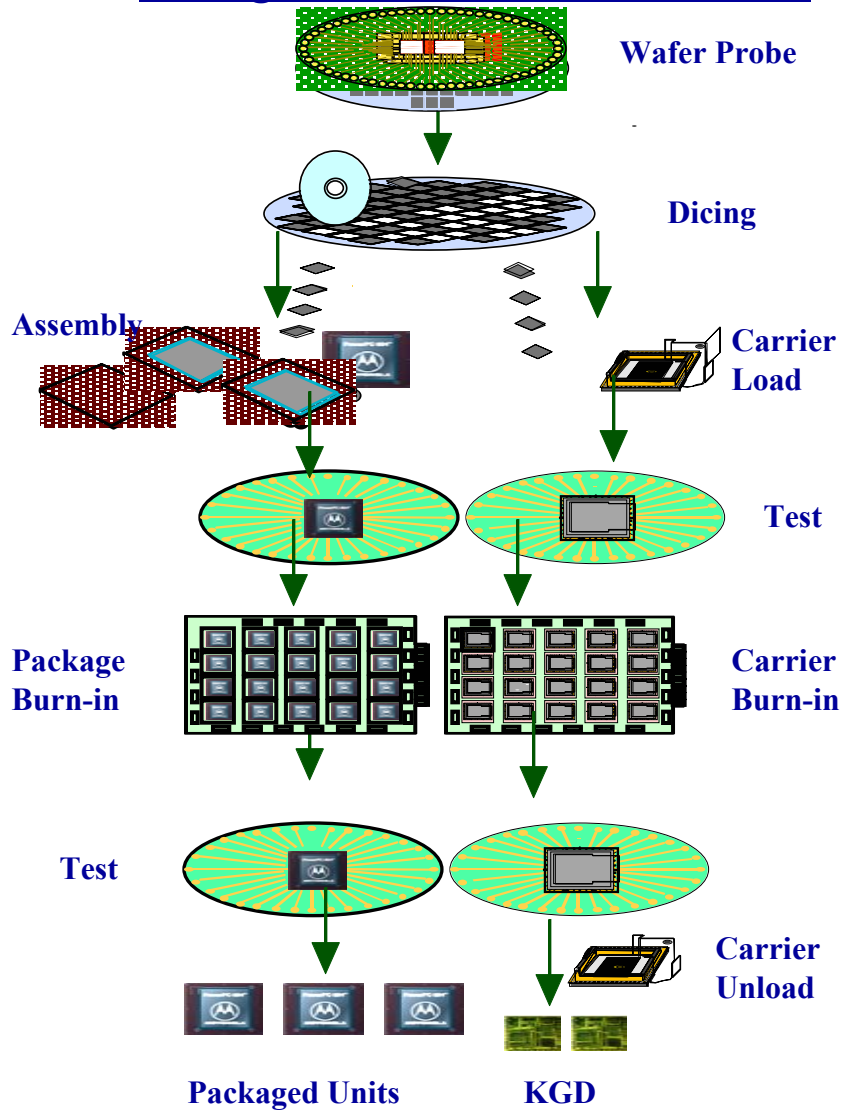
Why WLBT?

- **Smaller form factor requirements in personal communication, computer and automotive markets have increased demand for KGD.**
- **Burn-in for KGD at wafer level requires less test insertions and reduces cycle time than die level burn-in. Similar cycle time reductions can also be realized for package devices by screening out early life failures before assembly.**
- **WLBI provides quicker feedback to wafer factory, which improves responsiveness to provide more effective process control.**

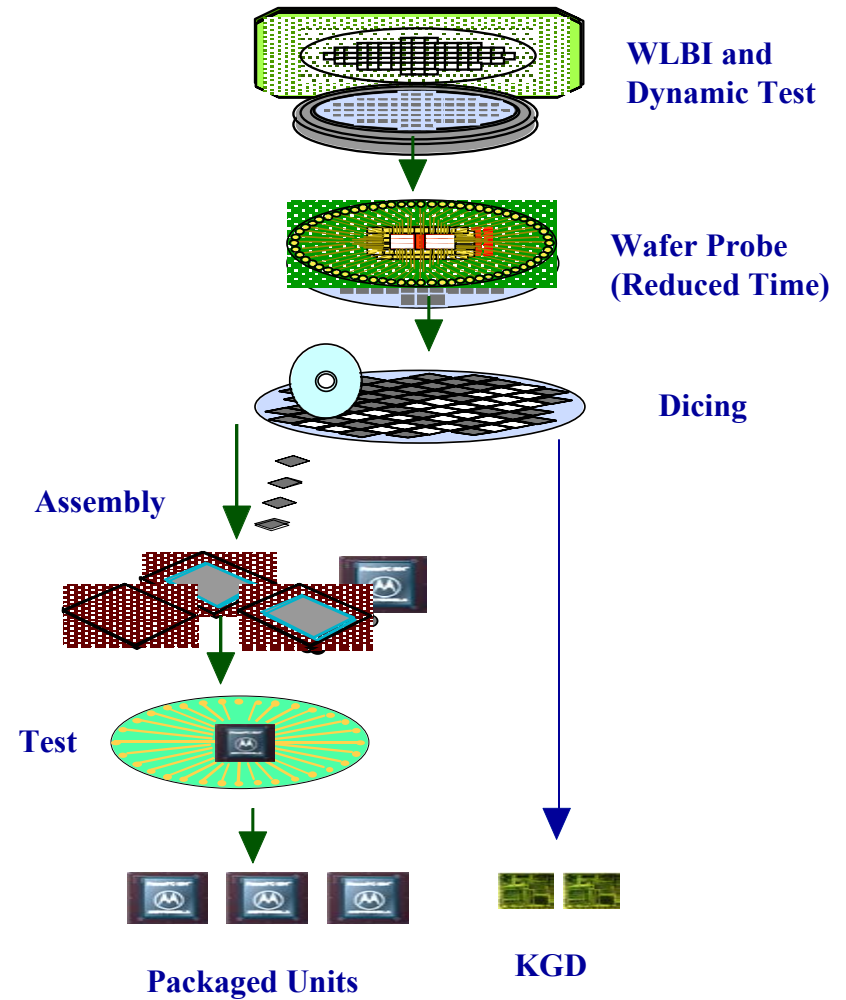


Wafer Level Burn-in Methodology

Package Burn-in / Die-Level Burn-in



Sacrificial Metal Wafer Level Burn-in



Cost Comparison Between Sacrificial Metal Wafer Level Burn-In and Test vs. Package Burn-In and Test
 9th Annual International KGD
 Packaging and Test Workshop; Napa, California
 W, Ballouli and T. McKenzie; September 8 - 11, 2002

Primary Attribute Differences*

Assume 360 die per wafer. Process 28 wafers or 10,080 devices per run.

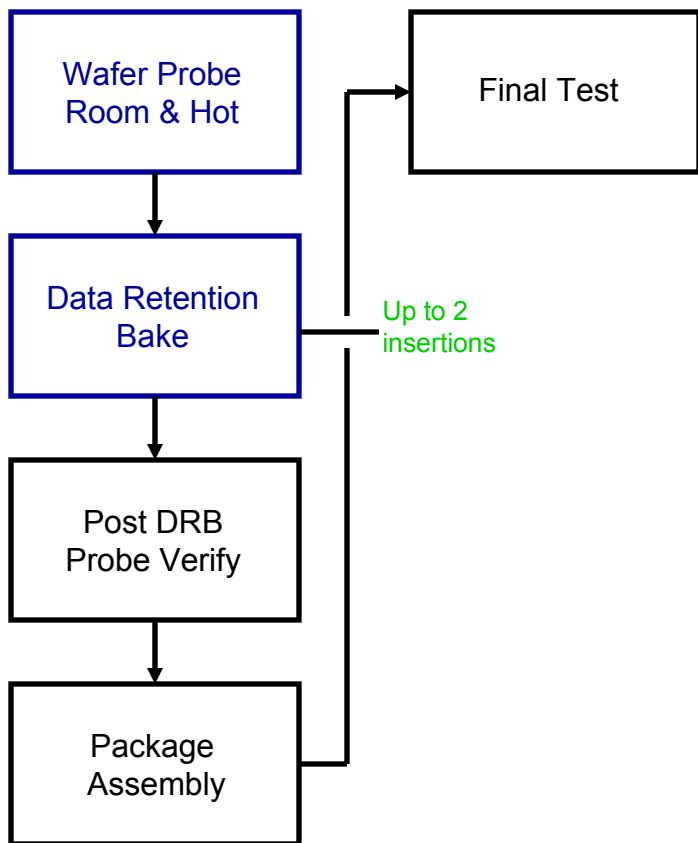
	<u>SM WLBT</u>	<u>Pkg Burn-In and Test</u>
# of Test Systems	1	7
# of Test Fixtures	28	360
Floor Area (sq ft)	90	210
System Thermal Dissipation	12 kW	21 kW

* Information provided by Delta V Instruments

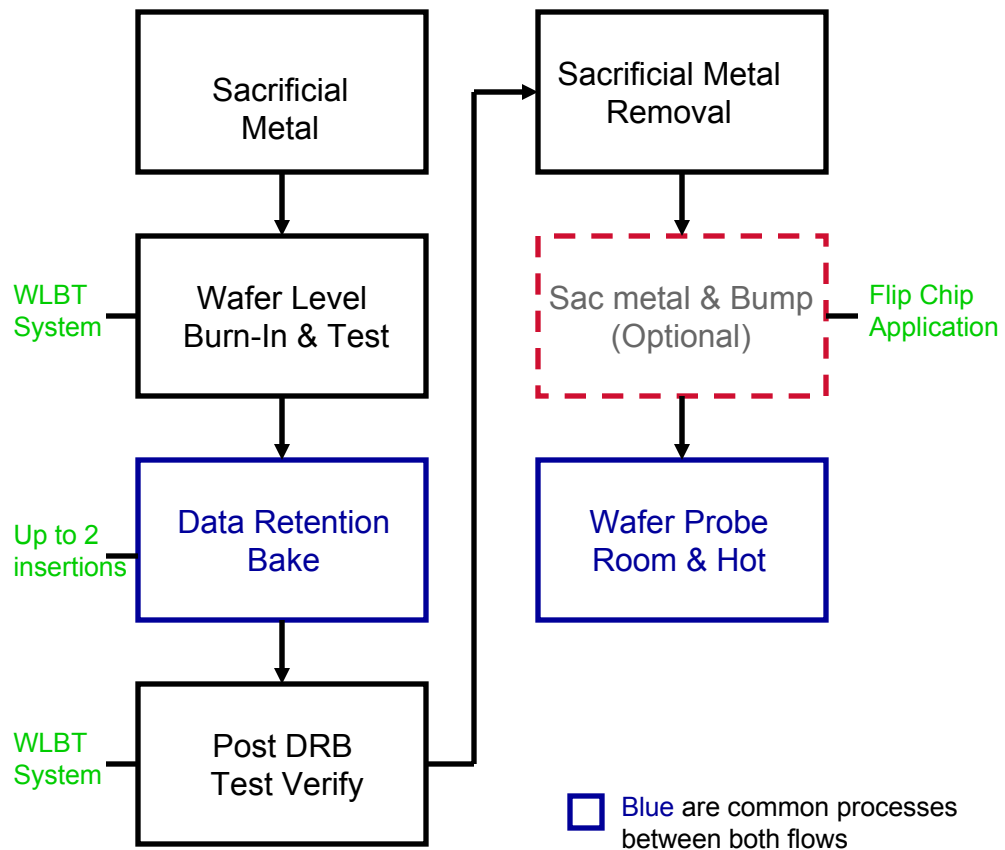


Process Flow Differences

Standard test and assembly flow



Sacrificial Metal Wafer Level Burn-in/test and bump flow



Package Burn-In Cost Attributes

- **Wafer Probe**

As charged by the factory – Mainly driven by test time

- **Data Retention Bake (optional)**

As charged by the factory

- **Package and Assembly**

Package type, Assembly, and Yield

- **Test**

As charged by the factory – Mainly driven by test time

- **Burn-In**

Burn-In Equipment and BI time

- **Post Burn-In Test**

As charged by the factory – Mainly driven by test time



Package Cost Analysis Equations

In This exercise we normalize package cost to the wafer level to provide proper cost comparison between package vs. KGD cost for backend process

- ✓ Total Wafer Assembly Cost = WAC

$$\mathbf{WAC = PAC * PDPW * WPY}$$

Where; WPY = Probe Yield, PDPW = Possible Good Die Per Wafer, PAC = Package Assembly Cost

- ✓ Total Wafer Package BI Cost = WPBIC

$$\mathbf{WPBIC = PDPW * PAY * PBIC}$$

Where; PAY = Package Assembly Yield, PBIC = Package Burn-In Cost

- ✓ Total Wafer Final Test Cost (package test) = WFTC

$$\mathbf{WFTC = PDPW * WPY * PAY * PFTC}$$

Where; PFTC = Package Final Test Cost

- ✓ Total Wafer Cost = TWC

$$\mathbf{TWC = WPC * WAC * WPBIC * WFTC}$$

Where; WPC = Wafer Probe Cost

- ✓ Total Package Cost = TPC

$$\mathbf{TPC = TWC / GPPW}$$

Where; GPPW = Good Package Per Wafer



SM WLBT Cost Attributes

✓ Sacrificial Metal Deposition and Pattern

Sputter, Photo, Etch, and Strip Process Equipment and Materials

✓ Wafer Level Burn-In and Test

Test Equipment

Test Fixtures

Up to two insertions (DRB “1”s and “0”s)

✓ Data Retention Bake (optional)

✓ Sacrificial Metal Strip

✓ Bump (optional)

✓ Probe

✓ Tape and Reel



WLBT Analysis Equations

In This exercise we normalize KGD cost to the wafer level to provide proper cost comparison between package vs. KGD cost for backend process

- ✓ Good Die Per Wafer after WLBT = GDPW2

$$\mathbf{GDPW2 = PDPW2 * WPY2}$$

Where; PDPW2 = Possible Good Die Per WLBT, WPY2 = WLBT Probe Yield

- ✓ Die Lost due to WLBT Implementation = DLWI

$$\mathbf{DLWI = AGDPW - PDPW2}$$

Where; AGDPW = Anticipated Good Die Per Wafer (past probe, no WLBT)

- ✓ WLBT Cost Adder = WCA

$$\mathbf{WCA = DLWI * PSP}$$

Where; PSP = Package Sales Price

- ✓ Total Wafer Cost (WLBT) = TWC2

$$\mathbf{TWC2 = WLBTC * WCA * WPC2}$$

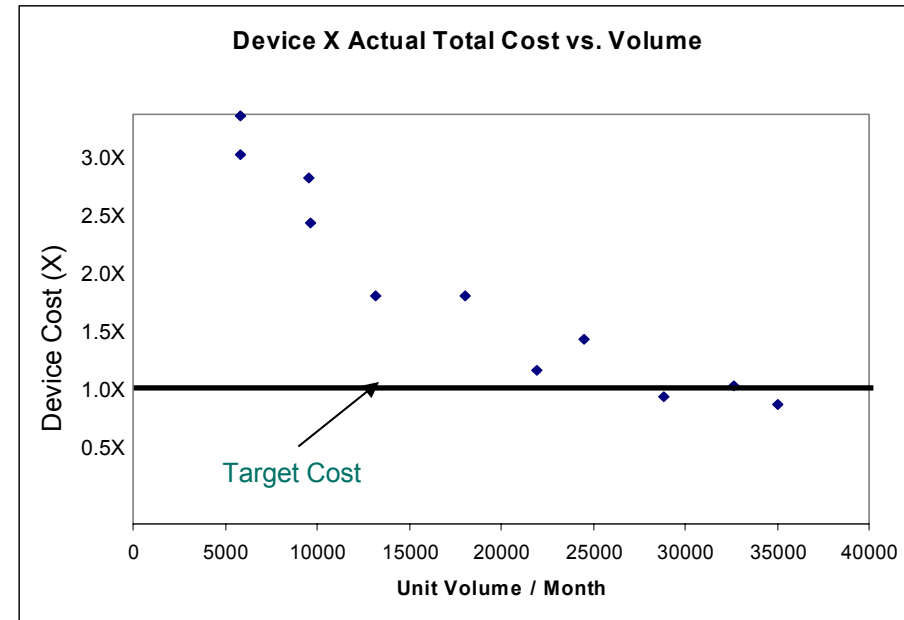
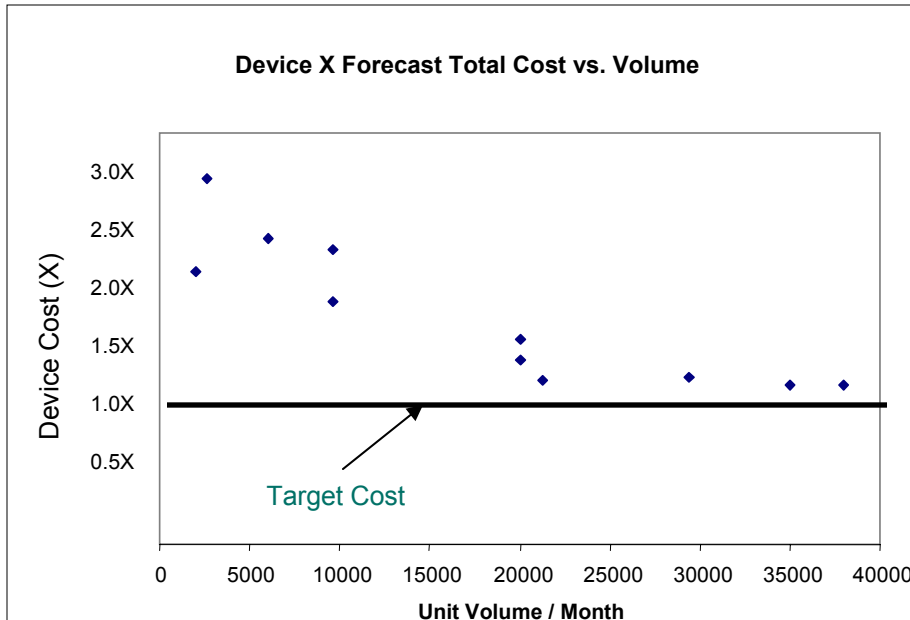
Where; WLBTC = WLBT Cost (includes Sac. Metal and BIT), WPC2 = Wafer Probe Cost

- ✓ Known Good Die Cost = KGDC

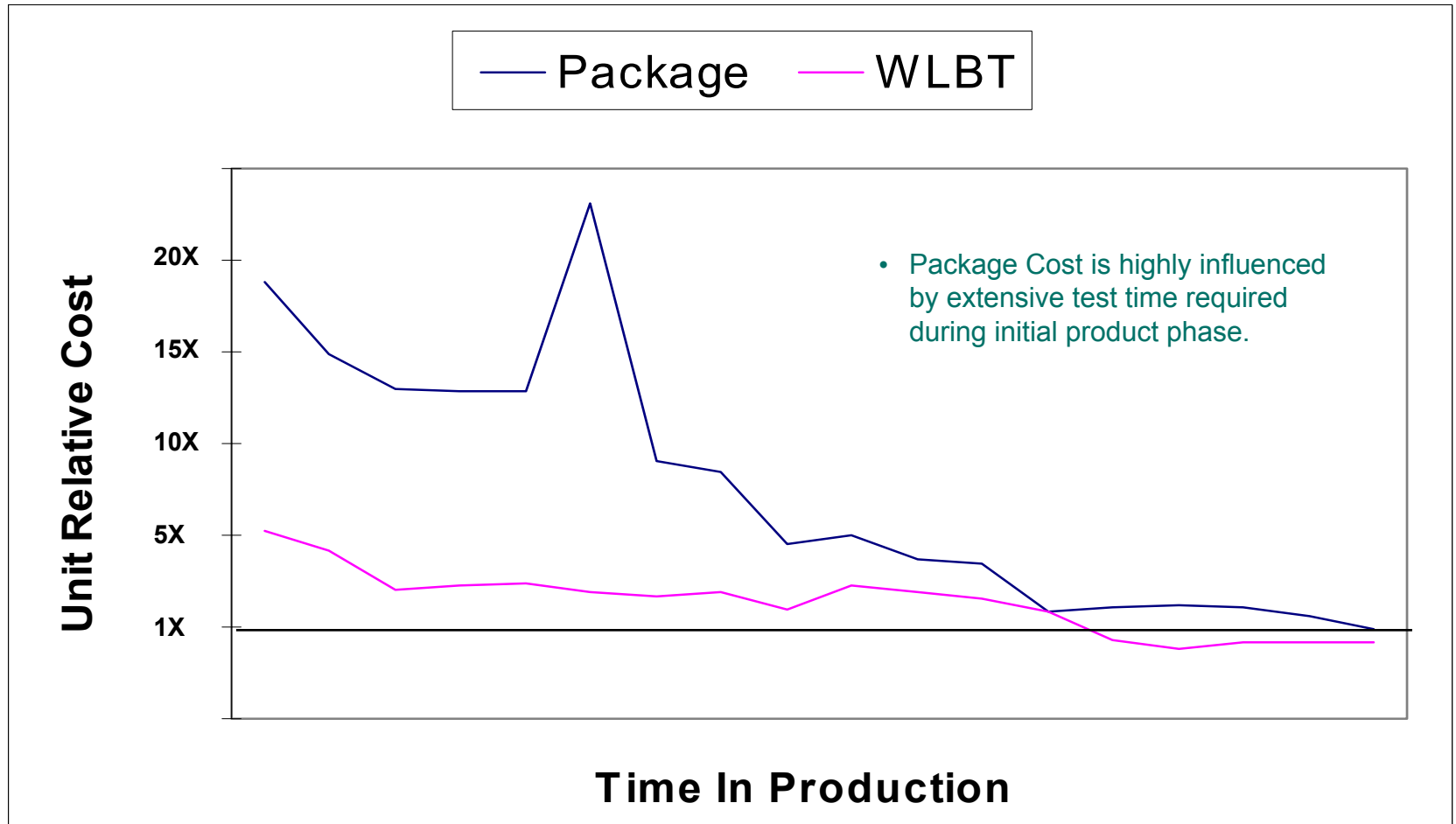
$$\mathbf{KGDC = TWC2 / GDPW2}$$



SM WLBT Forecast vs. Actual Cost



Total Unit Cost (Package vs. WLBT)



Summary

Sacrificial Metal Wafer Level Burn-in and Test

- **Sacrificial metal wafer level burn-in is a low cost test solution to achieving known good die.**
- **Motorola has been in production utilizing this technology since 1995.**
- **High cost test equipment and floor space requirement resulted in relative WLBT cost improvement as compared to package cost**



Acknowledgments

This speaker would like to acknowledge the teamwork from various Motorola SPS groups, Delta V Instruments, and Despatch Industries that contributed to the development and continuous improvement of this Sacrificial Metal Wafer Level Burn-in and Test program.



Reference Articles

- **W. Ballouli and T. McKenzie, “Design For Sacrificial Metal Wafer-Level Burn-In”, 2001 EtroniX (Advanced Packaging) Conference, February 2001 (articles on CDROM).**
- **W. Ballouli, T. McKenzie, and N. Alizy, “Known Good Die Achieved Through Wafer-Level Burn-In and Test”, 26th IEEE/CPMT IEMT Symposium, October 2000, pp. 153-159.**
- **W. Ballouli, C. Beddingfield, F. Carney, and R. Nair, “Wafer-Level KGD Technology for DCA Applications”, *Advanced Packaging*, September 1999, pp. 26-30.**
- **T. McKenzie, “Wafer Level Burn-in (WLBI) Workshop”, Motorola Internal Publication, November 5, 1997.**
- **W. Ballouli, J. Stroupe, “TSM Approach to Wafer Level Burn-in”, Motorola Internal Publication, Motorola AMT Symposium, January 25, 1995.**

