True IDDQ Test and its Real-Life Application - Experiences and Targets from the Field

Dr. Hans Manhaeve
Q-Star Test nv.

Overview

- Setting the Scene
  - True IDDQ
  - IDDQ and Deep Submicron
- Practical examples of True IDDQ application
- An alternative IDD application
  - Power & Ground pin continuity checking

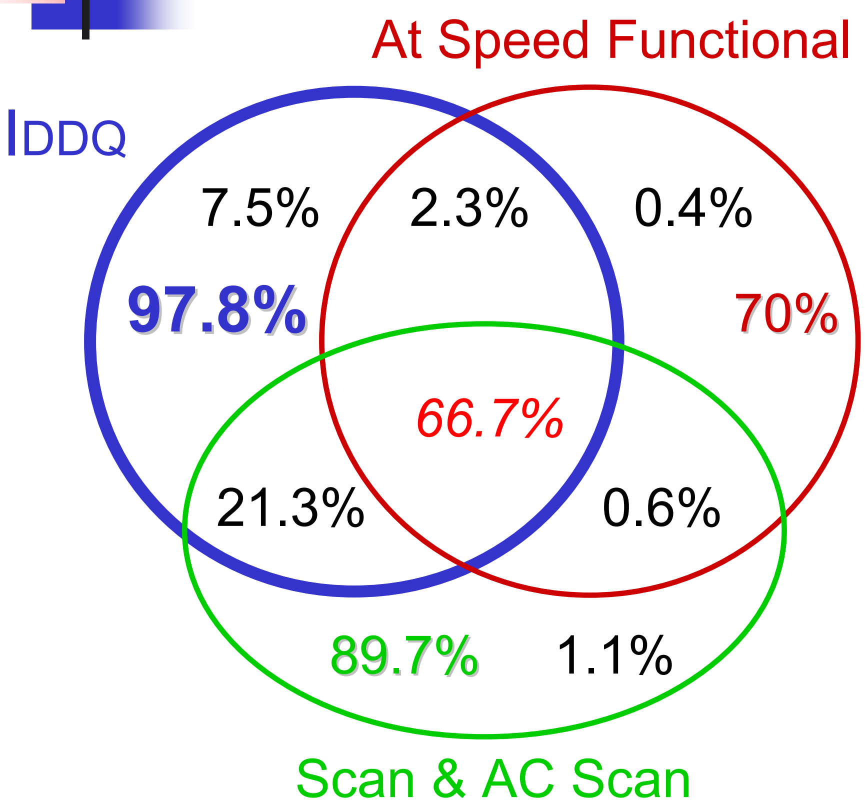
True IDDQ ?!

- Traditional IDDQ Approach:
  - All measurements are compared against a single threshold
  - Limited #measurements (1-10) due to economical (test time) constraints (limited coverage)
  - IDDQ is seen as a quality related "add-on"
- True IDDQ:
  - Not necessary a single threshold
    - Vector related – DUT related (adaptive limit setting)
  - IDDQ vector set with high fault coverage (> 90-95%) resulting in a "high" number of measurements (50-100-…)
    - Economical contraints are fading with available monitors
  - Not necessary an "add-on" but also (partly) replacement

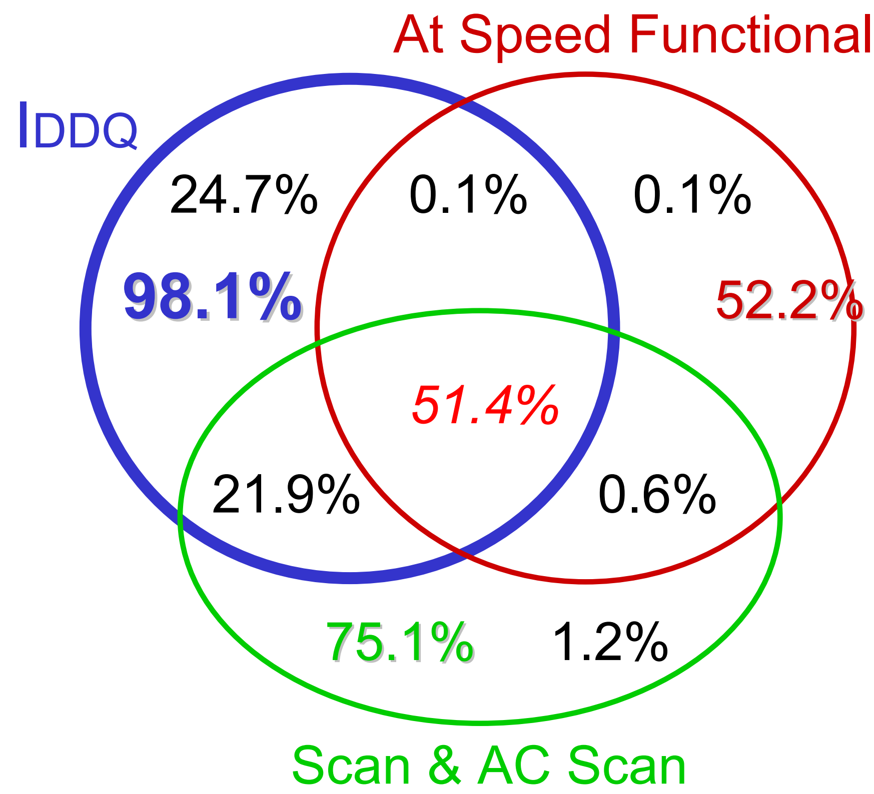
True IDDQ

- What does if offer:
  - Reduction of test pattern generation effort
    - Reduced number of ATPG vectors compared to S@ based scan
    - Ease of TPG generation (less demanding on ATPG tool resources)
  - Reduction on ATE memory requirements
    - Extending ATE lifetime before upgrading/replacement
  - Reduction of overall test time
  - Improvement of product quality
  - Improvement of Productivity

Some Data …



HP Data



IBM Data

> 100 IDDQ vectors

What about DSM ?

- Statements :
  - Scaling effects cause increase of leakage
  - Increased parameter variabilities for deep sub-micron might mask defect currents
- Questions :
  - Is I_{DDQ} testing only a Hype ? NO
  - Will I_{DDX} testing drown in the Deep Sub-micron Leackage Ocean ? NO
  - Is there an I_{DDX} Test Future ? YES

What says the Roadmap?

Year	1999	2000	2001	2002	2003	2004	2005
Technology	180nm	165nm	150nm	130nm	120nm	110nm	100nm
Ioff max, LP (pA/µm)	5	7	8	10	13	16	20
Wn (µm)	2.5	2.3	2.1	1.9	1.7	1.6	1.4
Wp (µm)	5.0	4.5	4.1	3.8	3.4	3.1	2.8
Ioff LP (1Mtran) (µA)	4.688	5.966	6.198	7.044	8.324	9.314	10.584
#Transistors (M)	4	8	16	32	64	128	256
Ioff LP (µA)	18.75	47.73	99.17	225.39	532.75	1192.17	2709.47
Wn (µm)	0.5	0.5	0.4	0.4	0.3	0.3	0.3
Wp (µm)	1.0	0.9	0.8	0.8	0.7	0.6	0.6
Ioff LP (1Mtran) (µA)	0.938	1.193	1.240	1.409	1.665	1.863	2.117
Ioff LP (µA)	3.75	9.55	19.83	45.08	106.55	238.43	541.89

Solutions for DSM

- Design solutions
  - Low power design requirements and power management support further use of I_{DD} tests
  - Use of built-in current monitors
  - RBB – FBB – Stacked transistors – dual V_T
- Measurement solutions
- Process solutions
  - cfr press releases by Intel & others

Solutions for DSM

- Measurement Solutions:
  - Delta-IDDQ
    - At least applicable for IDDQ upto 100mA (Philips ITC'2001)
    - A variety of delta approaches are existing
      - Vector to vector, die to die, …
  - Current Signatures
  - Current Ratios (HP, ITC'1999)
  - Transient Current Testing (IDDT)
  - Combined IDDQ – IDDT testing

Solutions for DSM

- Relative IDDQ:
  - Independent on leakage levels & process spreading
  - The background:
    - Background leakage as well as its variability from die to die are increasing due to
      - Technology
      - Increased design complexity

      → imposing limit setting problems
    - Matching Theory
      - Increasing design complexity (more transistors) results in a better matching of the state dependent leakage currents. This effect results in a reduced vector to vector IDDQ variation for a single IC, and compensates at least partially, maybe fully, the increase in variability of leakage currents from transistor to transistor when transistor dimensions are reduced in each new IC technology generation.

Solutions for DSM

- Relative IDDQ:
  - The approach
    - DUT related
    - Based on taking the ratio of a measurement with a reference measurement
    - Good devices: IDDQ ratio ~ 1
    - Defective devices: IDDQ ratio >> 1 or << 1
  - Requirements
    - Current measurements with high resolution and high repeatability

Solutions for DSM

- Relative IDDQ:
  - The advantages:
    - Easy to determine pass/fail criteria
    - High accuraccy of pass/fail decision
    - Technology independent. Easily applicable to new technologies and new products.
    - Relaxed IDDQ testability requirements: additional sources of leakage currents in the IC are allowed, as long as they are stable in time.
    - During production test: minimal data processing and immediate pass/fail decision.

Experiences from the Field

Example : IBM

- IDDQ is standard part of today's test flow
- Typically: 6 – 12 measurements
- Moved from "Traditional" to "Delta" IDDQ
  - To accommodate for technology related increased leakage
  - Delta approach: Vector-to-vector delta with combined delta/absolute limit.

  - Source: 4th European Manufacturing Test Conference – Semicon Eu

Case Study 1: European IC Manufacturer

Q-STAR TEST
The Current Test Company

- Project Objectives:
  - Evaluate performance & ease of use of loadboard monitor solutions
  - Pave the pathway for DSM I_{DDQ} test applications and the use of advanced I_{DDQ} test strategies.
  - Reduce overall test costs
- Test vehicle:
  - 0.18µm CMOS, >400k gates

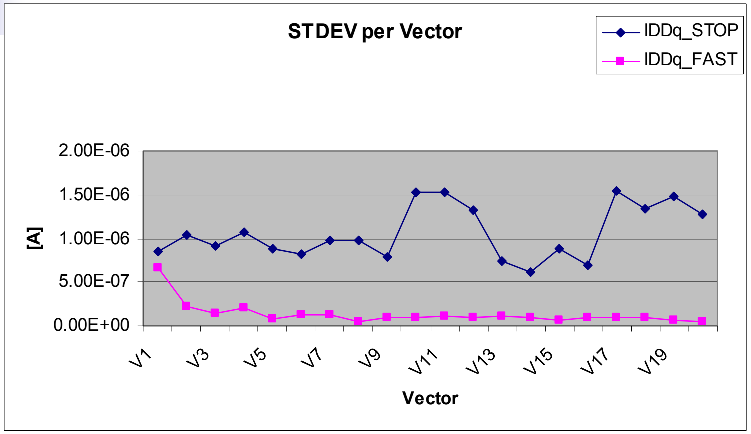
Case Study 1: Validation Setup

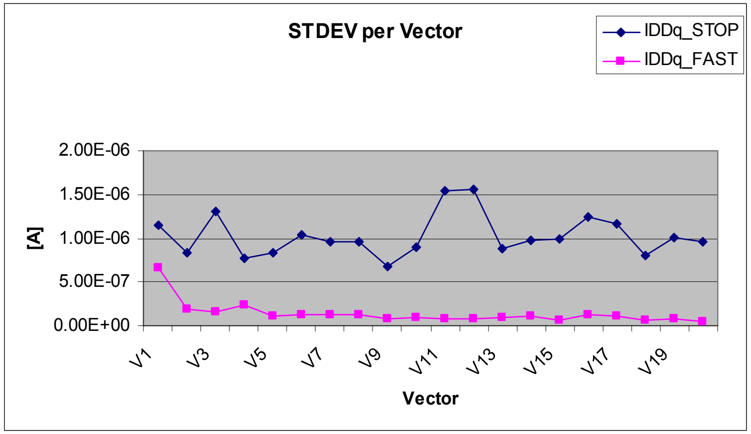
- ATE: Catalyst
- ATE measurement resource specs:
  - matrix source
  - 2mA range, 14 bit
  - Nominal resolution: 250nA
  - Accuracy: $\pm$ (0.1% measure + 1uA)
- Monitor measurement specs:
  - multiple threshold programmable module (QD-1010)
  - 1mA range, 16 bit
  - 4 samples > 90nA resolution

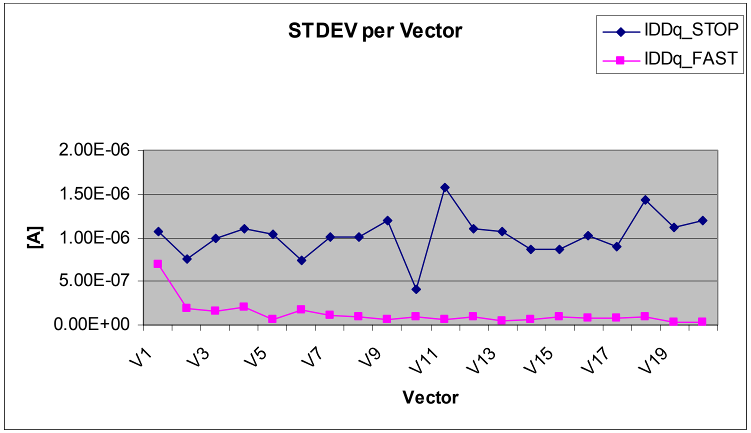
Case Study 1: Validation Results

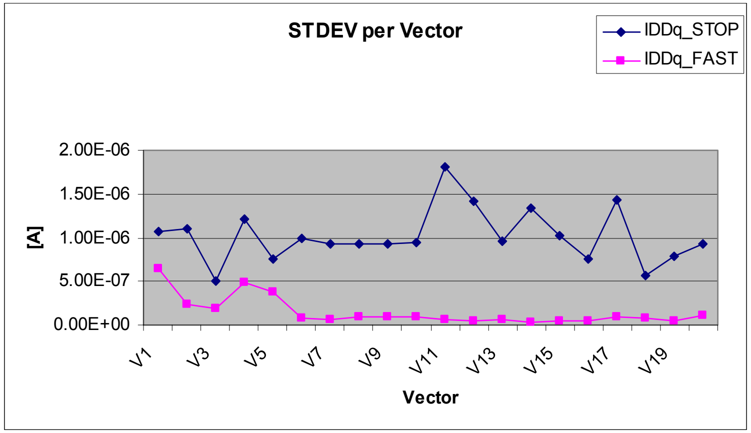
ATE

Monitor









Measurement repeatability, 20 strobes, 10 iterations per strobe

Case Study 1: Results

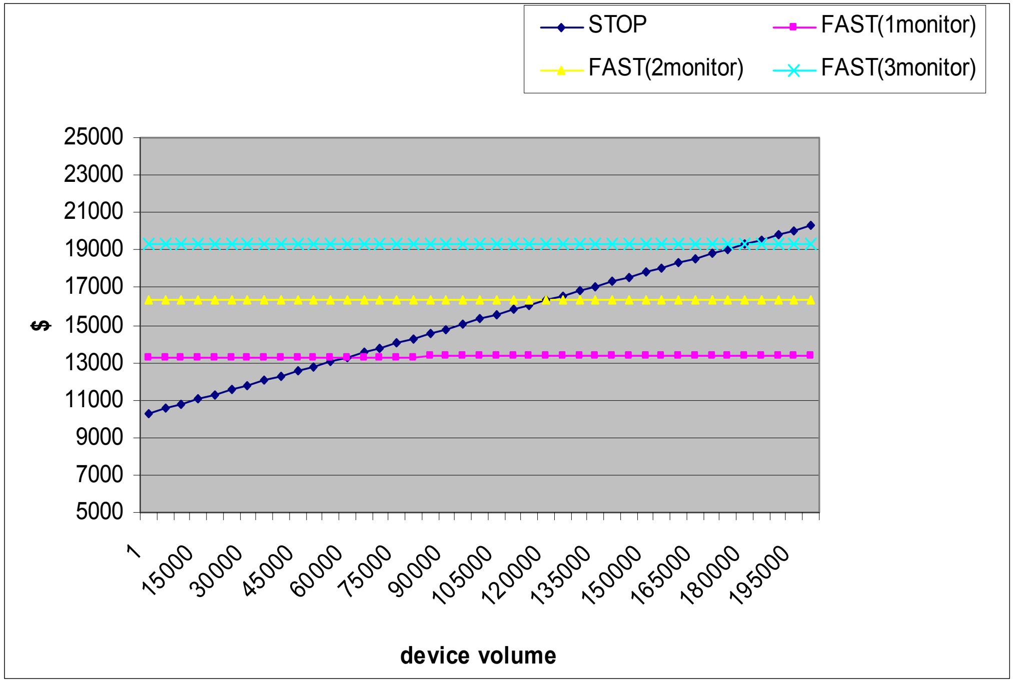
Measurement Time

	ATE	Monitor
# vectors	20	20
Coverage	92.1%	92.1%
Total test time	2724 ms	**4.84 ms**
Test Time per vector	136.2 ms	**242 µs**

STOP test time/ FAST test time ratio ~ 562

Case Study 1: Cost Analysis

- ATE fixed costs
  - Board development (HW)
  - Test prog. development (SW)
- Monitor fixed costs
  - Board development (HW)
  - Test prog. development (SW)
  - monitor



break-even points:

1 monitor ~ 60 000 devices
2 monitor ~ 120 000 devices

Case Study 1: Conclusions

- Significant test time reduction experienced which leads to considerable cost savings.
  - Short ROI
  - Enables further test optimisation
- Monitor resolution & data processing capabilities support DSM I_{DDQ} strategies
  - New projects will make use of monitor based I_{DDQ} methodology
- Automatic insertion of monitor control at TPG stage under preparation

Case Study 2: Motorola

- Project Objectives:
  - Evaluate performance & ease of use of loadboard monitor solutions
  - Increase wafer sort quality on basis of scan & enhanced I_{DDQ} tests
  - Reduce overall test costs
  - Pave the pathway for high quality tests using a low-cost DFT test platform.
  - I_{DDQ} Fault coverage >= 95%

Motorola

- Results:
  - #IDDQ vectors: 40 → 911 (x 23)
  - Total IDDQ test time:1.2s → 315ms (/4)
    - Measurement time: 30ms → 150µs / vector (/200)
  - Overall gain factor : ~92
  - Savings (test time only): 60k$/Mdev
    - + reduced die cost, reduced packaging cost, reduced FA costs, less field returns, …
  - Improved product quality
  - Pathway paved for Scan+IDDQ based test approach on low cost DFT platform

Other Results:

- Test Time reduction
  - 10 IDDQ meas./dev – ATE 80ms/meas : 800ms
  - Monitor: 100µs/meas, Savings: 799ms/dev
  - Test cost savings ~56k$/Mdev
- Quality Improvement
  - Pre: failure rate: >200ppm, few IDDQ vectors
  - Post: 80-100 IDDQ vectors, max 10ms IDDQ test time, failure rate <50ppm

Ongoing projects

- Vector Trade-off
  - Objectives:
    - Increase of overall defect coverage
    - Reduction of total test time
    - Reduction of test generation & test preparation efforts
  - Prerequisite
    - Fast IDDQ measurement solution
  - Approach:
    - Generate vectors for high (>95% IDDQ Cov)
    - Grade IDDQ vectors for S@ coverage
    - Generate S@ vectors for not yet covered faults

Ongoing projects
Strategy change on basis of Fast IDDQ

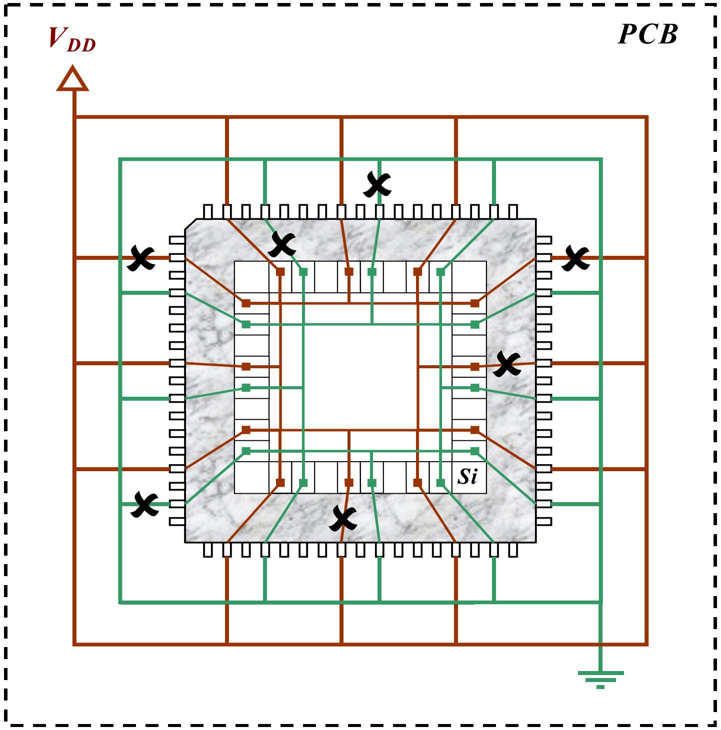
- MultiSide IDDQ testing
  - Objectives:
    - Increase test throughput, Total test time reduction, Minimize hardware requirements (DPS/PMUs)
  - Prerequisite
    - Dedicated multi-monitor module
- Test platform optimisation
  - Objective:
    - Overall test cost reduction on basis of equipment cost
  - Approach:
    - Wafer screening on low cost DFT system, high IDDQ fault coverage
    - Limited qualification tests on high performant ATE

Alternative I_{DD} application

Verification of IC Supply Connections

Supply Pin Continuity
The Need

- Deep Sub-Micron needs High Quality, Low Impedance power supply networks
  - # of supply pins is expected to explode for future ICs
    - Increasing power/performance demands
    - Increasing current demands
  - Limits on pin count require:
    - Limits on "spare" supply pins
    - Need for reliable connections
  - Board level failures cause reliability problems

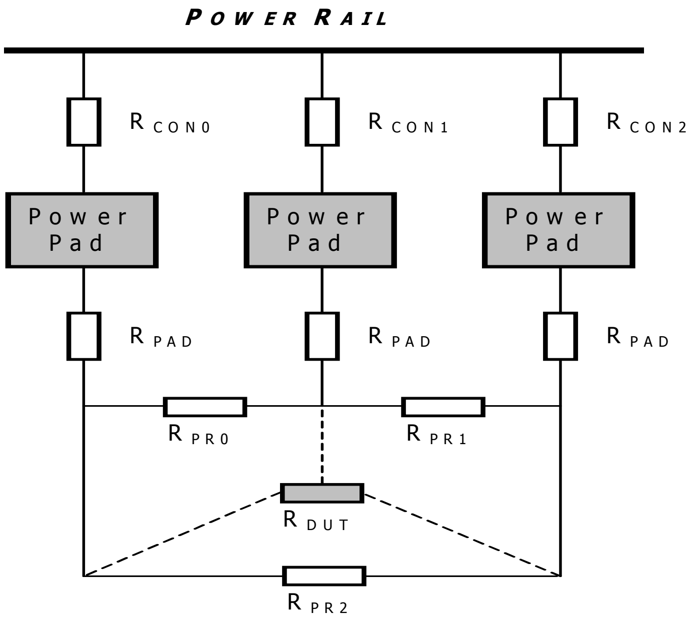


Supply Pin Continuity:
The Test Challenge

- The power distribution network : parallel network
  - A single failure only affects marginally overall characteristics
  - Measuring globally is impossible
    - Process variations mask the effects of a failing connection
- Solution
  - A dedicated test strategy & test circuit to verify each power supply pin individually, independent of parallel connections
- Existing solutions
  - Traditional vision verification techniques & the use of "standard" current monitors ($I_{DDQ/T}$) *do not* provide these characteristics

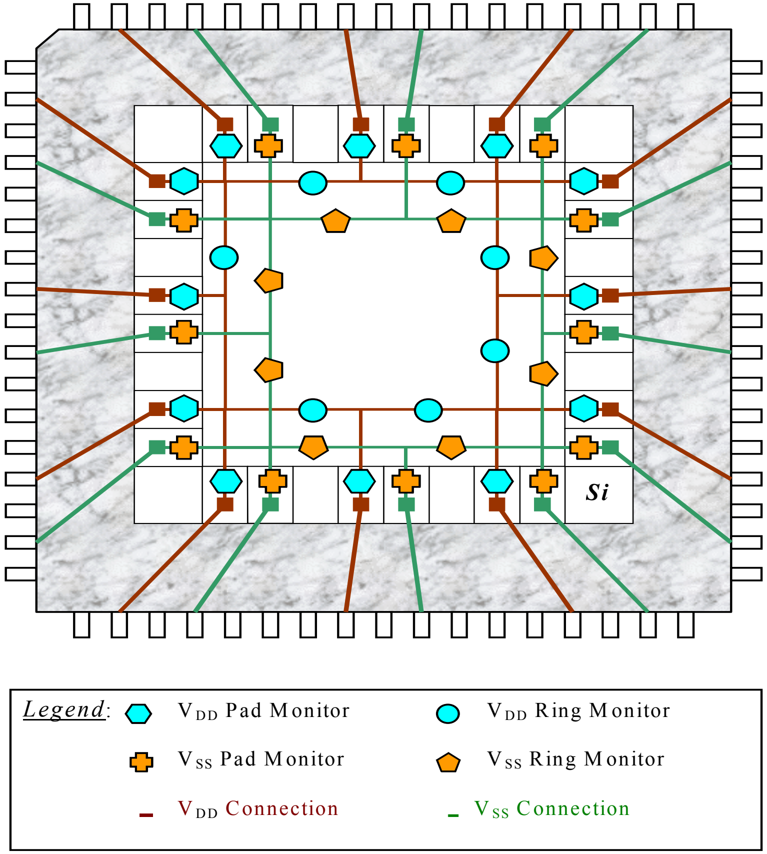
Test Methodology

- Detection of a (forced) current flow in the IC power distribution network
  - Controlled current sink placed at each pad-ring connection
- Uses voltage drop across inherent resistance of observed connection
- Current distribution:
  - *Good connection*
    - Most current via R_{PAD}
    - Small current via supply ring R_{PRx}
  - *Defective connection*
    - Most current via supply ring R_{PRx}
    - Small or no current via R_{PAD}



Test Methodology

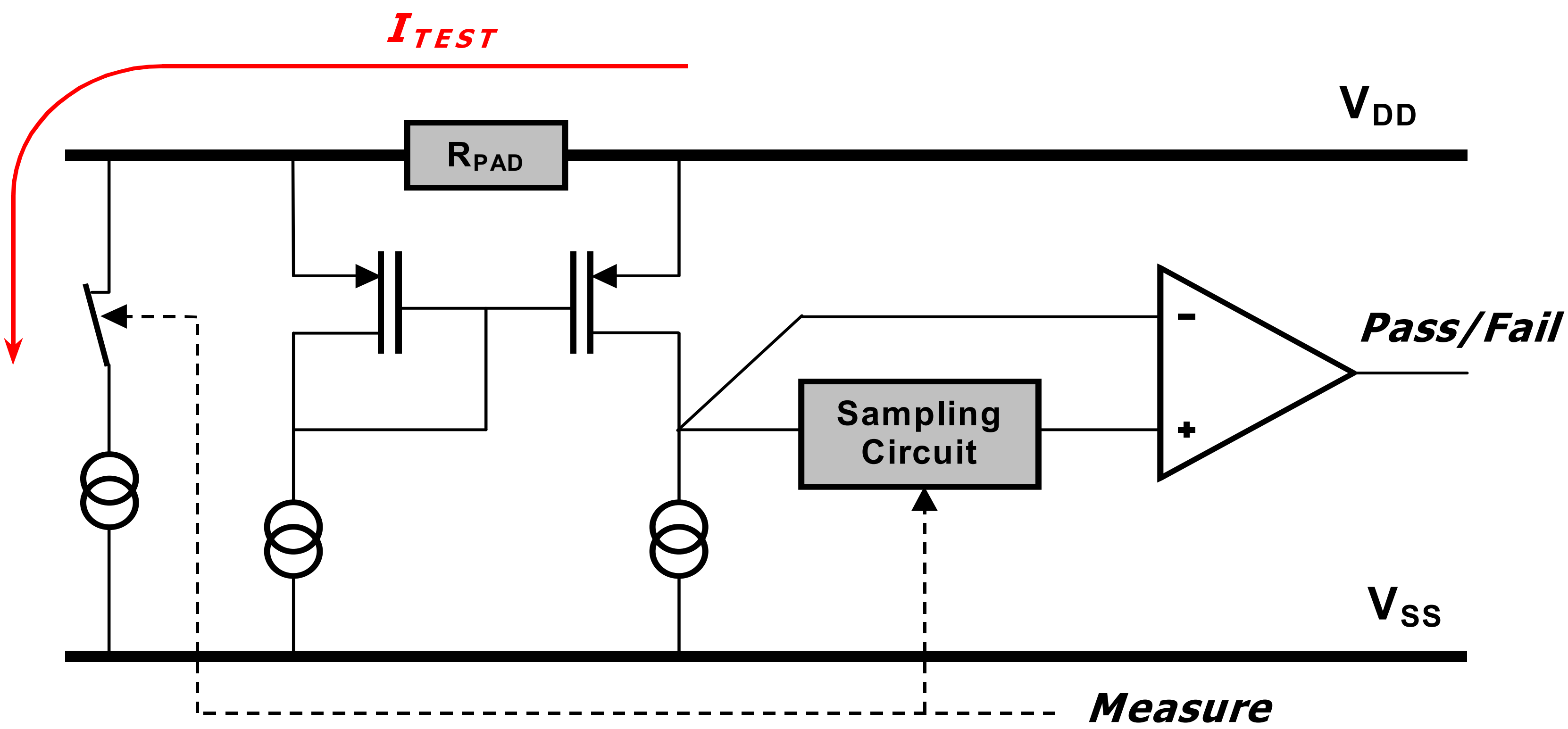
- Pass/Fail criterion
  - Variation of test current causes distinguishable voltage variation on pad and ring segments => useful pass/fail decision point
- Monitor types
  - Pad monitors
  - Ring monitors



Sensor *Requirements*

- Test circuit requirements
  - Not affecting the power & ground levels
  - Not affecting the CUT performance & operation
  - Easy to control, limited # of control pins
  - Power-down abilities
  - Sensor must be highly sensitive
    - Sense resistance is limited to 10 mOhms
  - No need for calibration
  - Reliable operation under different test conditions
  - High measurement repeatability

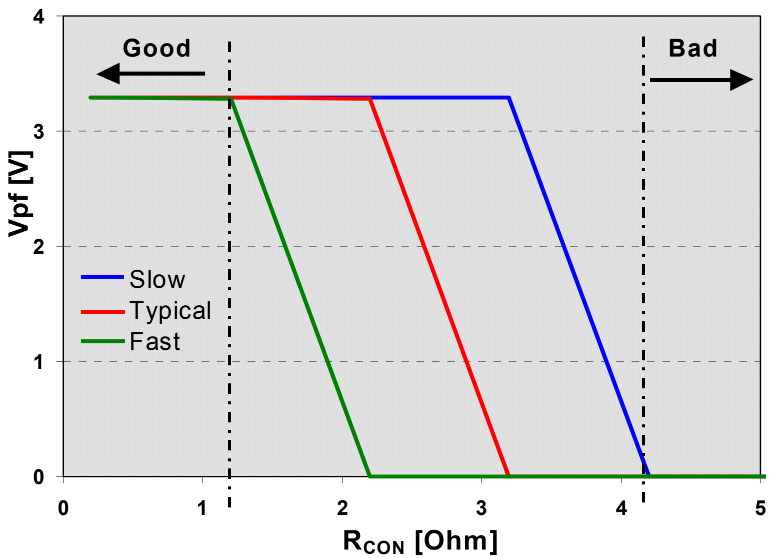
V_{DD} Pad Monitor
Block Schematic

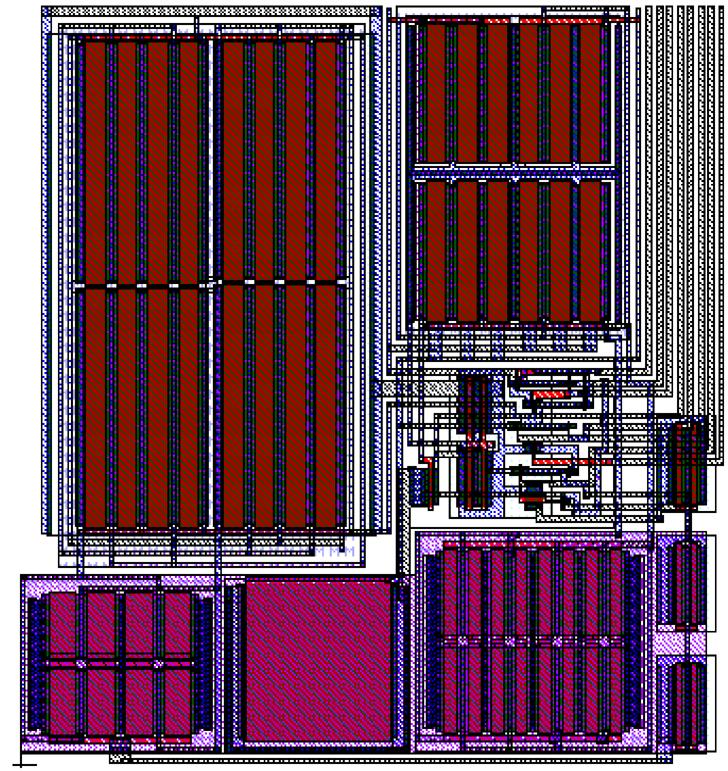


V_{DD} Pad Monitor

Layout

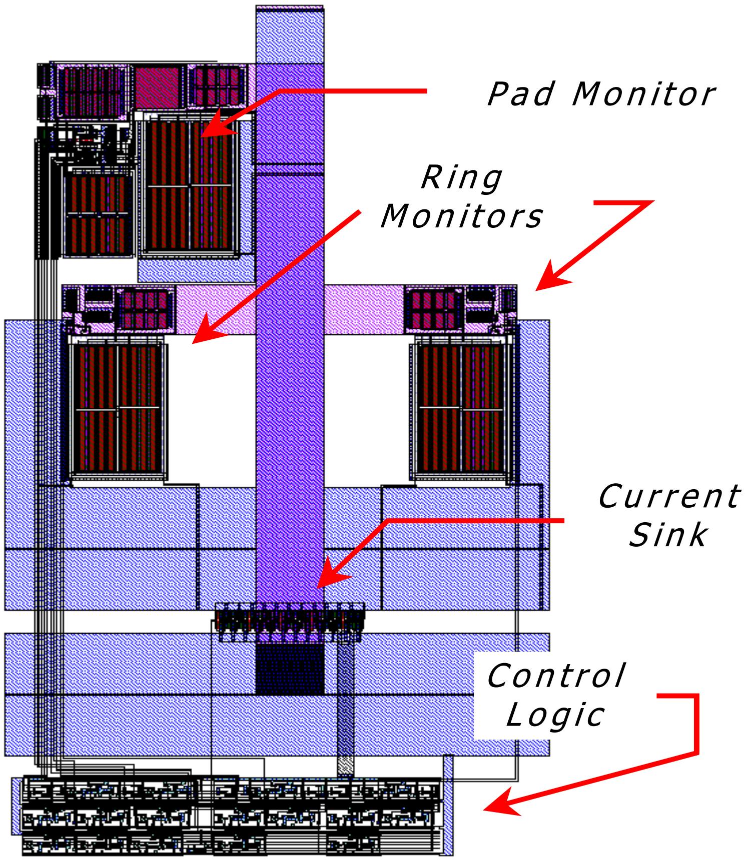
- Sensor is implemented in AµE 0.35µm CMOS technology
- Area: 95 by 100µm
- Only 2 metal layers used
- Bad contact if $R_{CON} \geq 1.5\ \Omega$





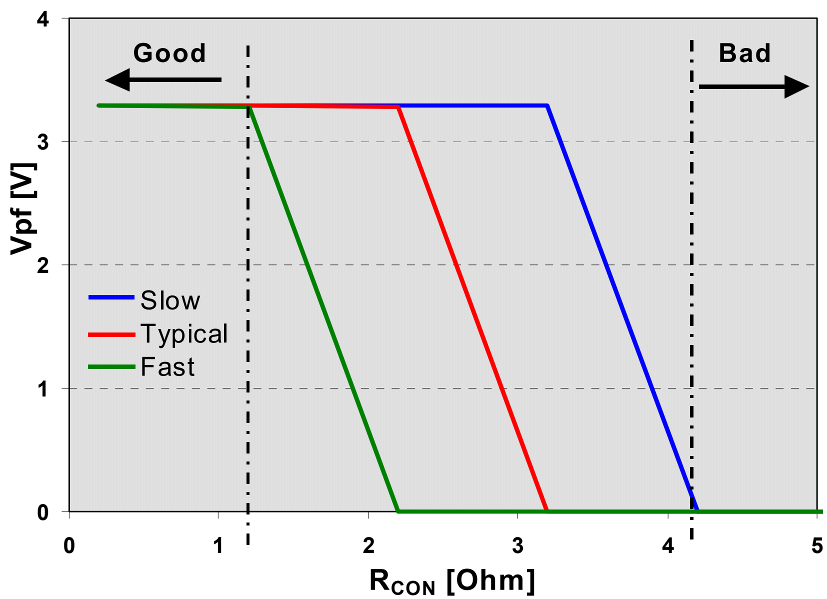
Test Chip Layout
V_{DD} / V_{SS} node

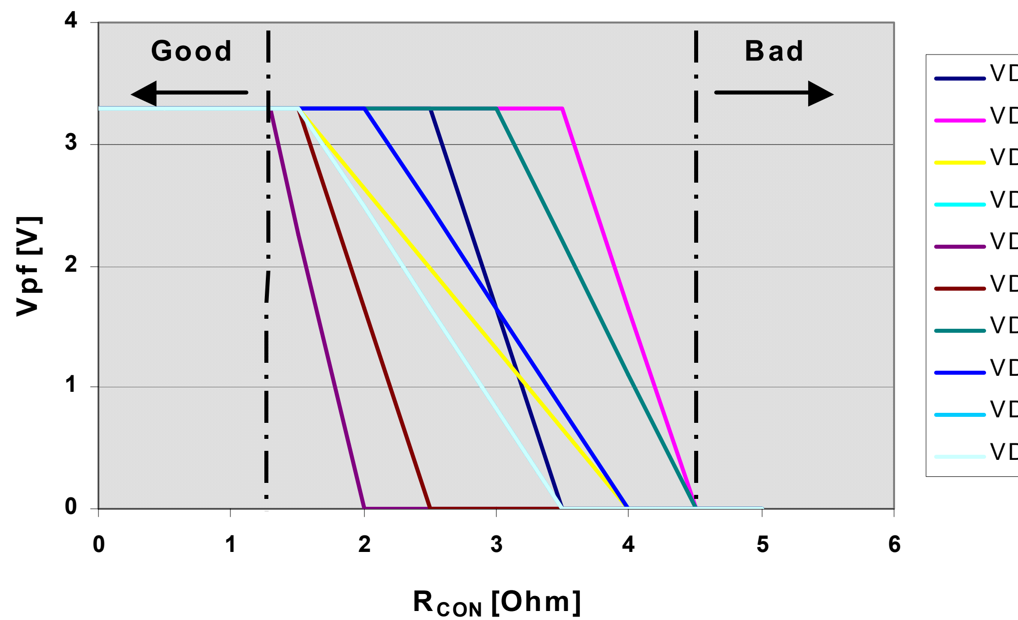
- V_{DD} Connection Node
  - 1 Pad monitor
  - 2 Ring monitors
    - Opposite polarity
    - Saturation operation
    - No differential architecture
  - Current sink
  - Control logic
    - Supporting multiple scan methods
- V_{SS} Connection Node
  - 1 Pad monitor + control logic



Test Results : *V_{DD} Pad Monitor*

- Comparison:
  - *Simulation* ⇔ *Measurement*





Project Summary

- Test Concept
  - Validated for V_{DD} power distribution network
  - V_{SS} network is not fully complementary
    - Bulk leakage
- Monitors are operational
  - V_{DD} pad monitor complies to all sensor requirements
  - V_{DD} ring monitor needs to be adapted to power distribution network
  - V_{SS} pad monitor operational but could not be fully characterised (~ test structure limitations)

Alternative Applications

- Power/Ground Verification at
  - Wafer Sort Testing
    - Verify if each power/ground probe makes proper contact => increase probe usable lifetime
  - Packed Device Level
    - Continuity checks for power/ground pins
- I/O pin Verification
  - When traditional approach (e.g. ESD diode test) fail
    - Analogue inputs and outputs
- Online, I_{DDQ} & I_{DDT} current testing
    - Requires modifying the detection circuitry

Conclusion

- True IDDQ testing offers a high potential for test cost (execution & capital spending) and test (preparation) effort reduction
- True IDDQ test application supported by proper software (ATPG) and hardware (monitors) tools
- Solutions exist and are applied for DSM
  - Need for paradigm shift from "Classical or Standard" to "DSM" IDDQ
  - Increased leakage is not "The" issue but "Data Handling" is the key