Test Flows for Consumer SiP

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Test Theory Background

Why Test

Test is about quality & the cost of delivering it given an imperfect manufacturing process.

- **Reduce defect rate at next level of assembly or use – Risk reduction**
  - Reduce scrap cost
  - Reduce customer failures
- **Provide information to improve the manufacturing process so that defect rate can be achieved with less effort – Yield learning**

Distribution of Test

- **Strategy at each level of assembly:**
  - – Detect defects caused by preceding assembly operation
  - – Verify component tolerances add up to working system thus far
  - – Diagnose defects caused by preceding assembly operation
- **Opportunity at each test insertion:**
  - – Different environmental conditions – T, V
  - – Different signal integrity
  - – Different equipment

Test Quality & Cost

- **No test is perfect**
  - – False positive (test escape): Bad part that is passed
  - – False negative (overkill): Good part that is rejected
- **Outgoing quality traded for test cost**
  - – Error cost: False Pos. > False Neg.
  - – Errors approach 0 asymptotically with test effort (time, # of vectors, # of instruments), i.e. test cost

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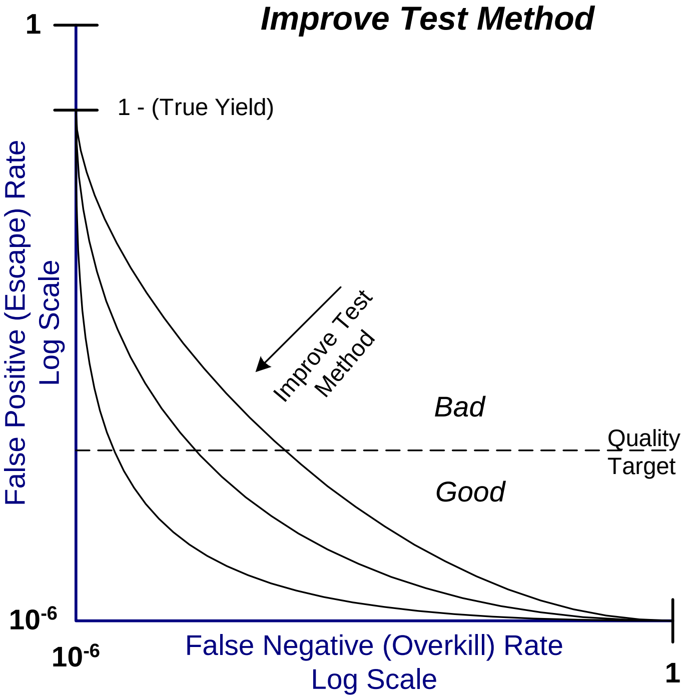
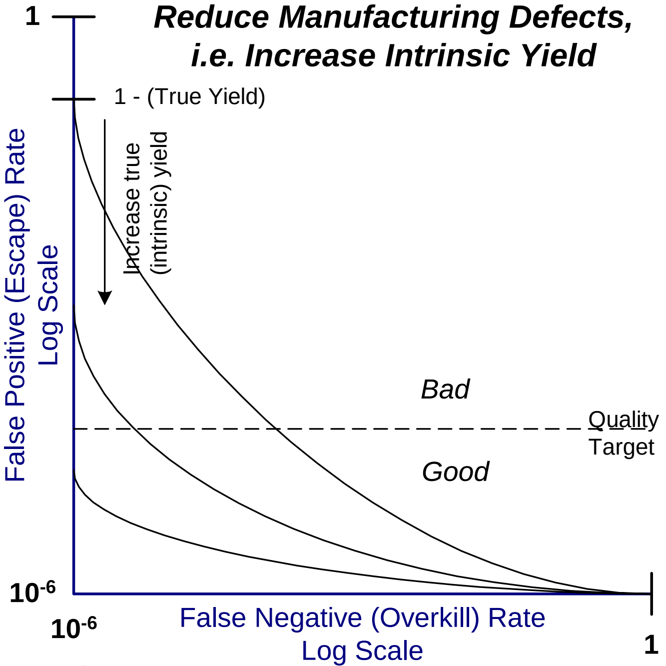
Test Effectiveness

- All tests trade false negatives for false positives but more explicit issue for DBT
- Trade-off varies widely with test method
- More square the curve, more effective the test method
- Mfg. defect density & quality target set effectiveness requirement
- Also trade test effectiveness, & resulting quality, for test cost


Improve Test Method


Reduce Manufacturing Defects, i.e. Increase Intrinsic Yield

Traditional Test Flow

	Wafer (Probe)	**Package (Final)**
Purpose	– Reduce defect rate to where packaging is economical – Fab yield learning	– Reduce defect rate to customer quality level – Assembly & some fab yield learning
Strategy	Find majority of die failures by low performance structural testing for catastrophic defects	– Find remaining, primarily parametric, die failures by functional performance testing – Serendipitously find assembly defects by same tests
Uniqueness	– Signal integrity usually worse than package – Opportunity for different conditions (T, V) – Easier parallelism	– High frequency & sensitivity – Opportunity for different conditions (T, V)
Multi-die challenge or opportunity	– Chips partitioned by function $\Rightarrow$ wafer tester may be specific to function – Yield compounding $\Rightarrow$ need more effective test	– Heterogeneous integration of diverse functions $\Rightarrow$ diversity of test methods, test times, tester resources, incoming quality – More effective die test $\Rightarrow$ need less effective pkg. test?

Mfg. Flow Defect Rate Breakdown

- **Final component requirement**
  - Customer will accept a few 100 ppm (5e-4)
  - Risks to avoid: repair cost, dissatisfied customer
- **Assembly process achievement**
  - Process defect rate is fraction of % (1e-3)
  - Too high to meet customer expectation ⇒ pkg. test required
  - Wafer test die defect escapes add to assembly defects
- **Wafer test requirement**
  - Die for *individual* die package (3e-2)
    - Risk to avoid – Cost of scrapped package & assembly effort
    - Economically allowed die defect level – few %
      - Too high to package test only for assembly defects
  - Die for *multiple* die package (3e-3)
    - Risks to avoid
      - Cost of scrapped package & assembly effort
      - Cost of scrapped good dice (yield compounding)
    - Economically allowed die defect level – fraction of %
      - Must be better than standard wafer test, but not as good as packaged
      - With true KGD, package test might only test for assembly defects

Economical Quality

Quality for Mobile Consumer

- **SiP growth being driven by mobile consumer products**
- **In contrast, concepts of die for SiP established by military, aerospace, automotive**
  - KGD: “As good as packaged”
  - No die testing or reliability screening required at subsequent levels of assembly
  - Implication of being “as close to perfect as practicable”
  - Defect rate < 100 ppm
- **Mobile consumer quality expectations**
  - Defect rate on order of fraction of %
  - Acknowledge the cost, willing to optimize cost & quality
  - Need to quantify cost & quality to optimize

Practical Approach to System Quality

- **Component quality matters because it affects yield (cost) of next level of assembly or customer experience**
- **Quality target at each level depends on factors such as:**
  - Customer expectations for specific application and market
  - Number, cost & quality of the other components
  - Cost & yield of assembly process
  - Cost of test
- **System integrator puts these factors into model of cost vs. quality, which he can run:**
  - Forward to see what his cost will be for particular set of components and assembly test processes
  - Backward to determine, for instance, level of die quality he needs to meet his cost and satisfaction goals
- **What system integrator needs from component suppliers:**
  - Measures of incoming quality to put in his model
  - Commitment to maintain quality level so that optimized mfg. & test flow remains so

New View of Die Quality

- **Goal – Know what more needs to be done to achieve application-specific quality target in a distributed test flow**
  - Good enough to meet finite end product quality level at near minimum cost
  - Know upper bounds on test escape rate, ELFR, LTFR
  - Know what’s been tested, and what hasn’t been tested but may yet need to be tested
  - Better than conventional probe but still cheap
- **New Term – *Die of Quality Known* (KQD)**
  - More than *Known Tested Die*
  - Way more than *Probed Die*

Specifying Die Quality

Digital

- **Escape Rate**
  - Fault coverage for each category – DPC spec.
    - Stuck-at
    - Transition
    - Path delay
  - Faults targeted & not targeted
  - Package test escape rate – sample of individually packaged dice, but sample is huge
- **Early Life Failure Rate (Reliability)**
  - Burn-in fail rate
  - Extrapolation from similar products in same process
  - Other screen fail rate

Analog/RF

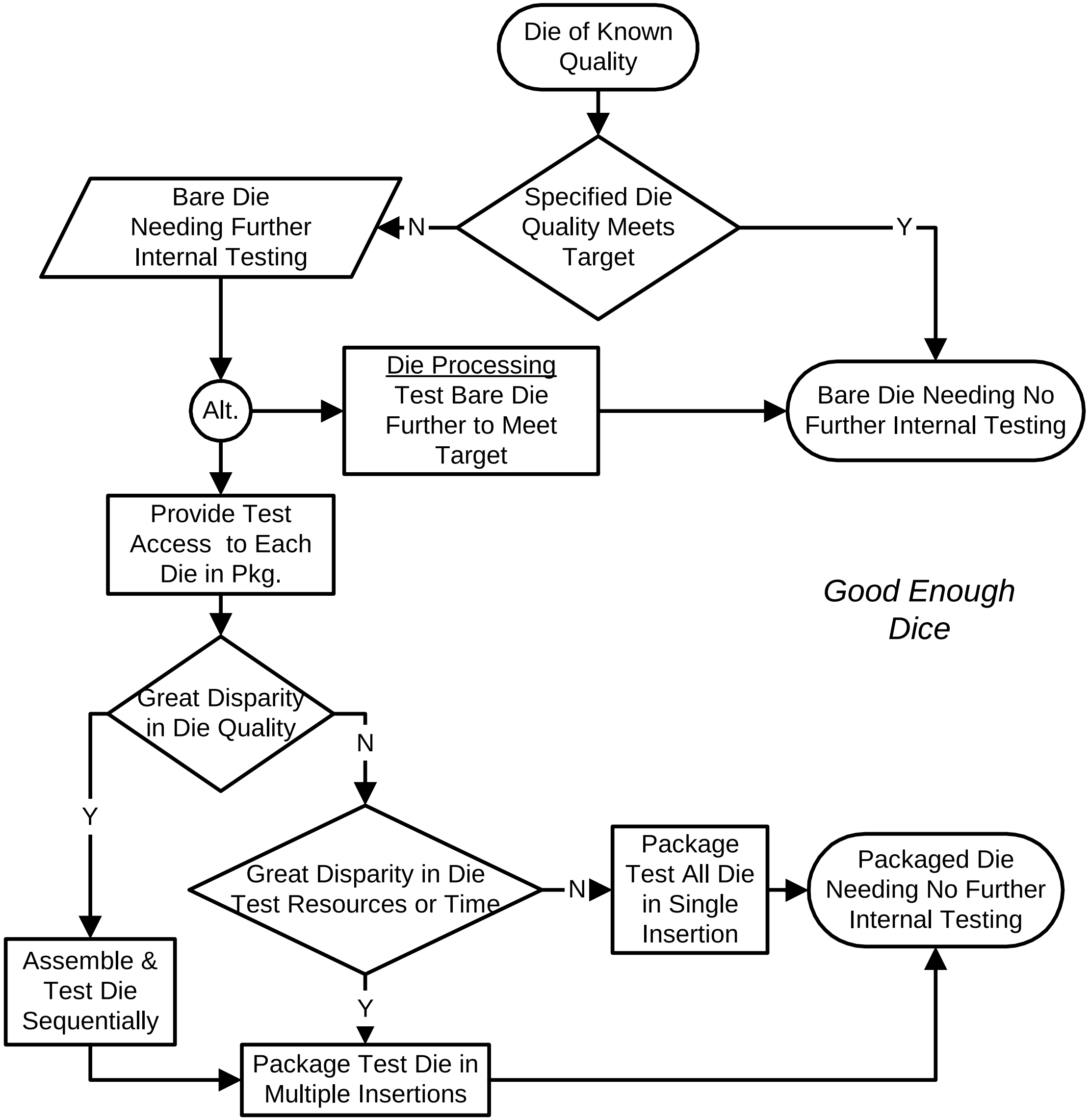
- **Escape Rate**
  - No practical fault model
  - MBT – Behavioral model fit error
  - Package test escape rate – sample of individually packaged dice, but sample is huge.
  - Extrapolation from similar products in same process
- **Early Life Failure Rate (Reliability)**
  - Burn-in fail rate
  - Extrapolation from similar products in same process
  - Other screen fail rate

Designing the Test Flow

Good Die

- Ideally use dice as received
- Bare die processing too expensive for consumer
- Possibly affordable alternative is to test die individually in package
- Disparities in quality, test resources, test time addressed by multiple insertions

- *But individually good dice & package may not play together - tolerancing*



Die of Known Quality

Specified Die Quality Meets Target

N

Y

Bare Die Needing Further Internal Testing

Alt.

Die Processing Test Bare Die Further to Meet Target

Bare Die Needing No Further Internal Testing

Provide Test Access to Each Die in Pkg.

Good Enough Dice

Great Disparity in Die Quality

Y

N

Great Disparity in Die Test Resources or Time

N

Y

Package Test All Die in Single Insertion

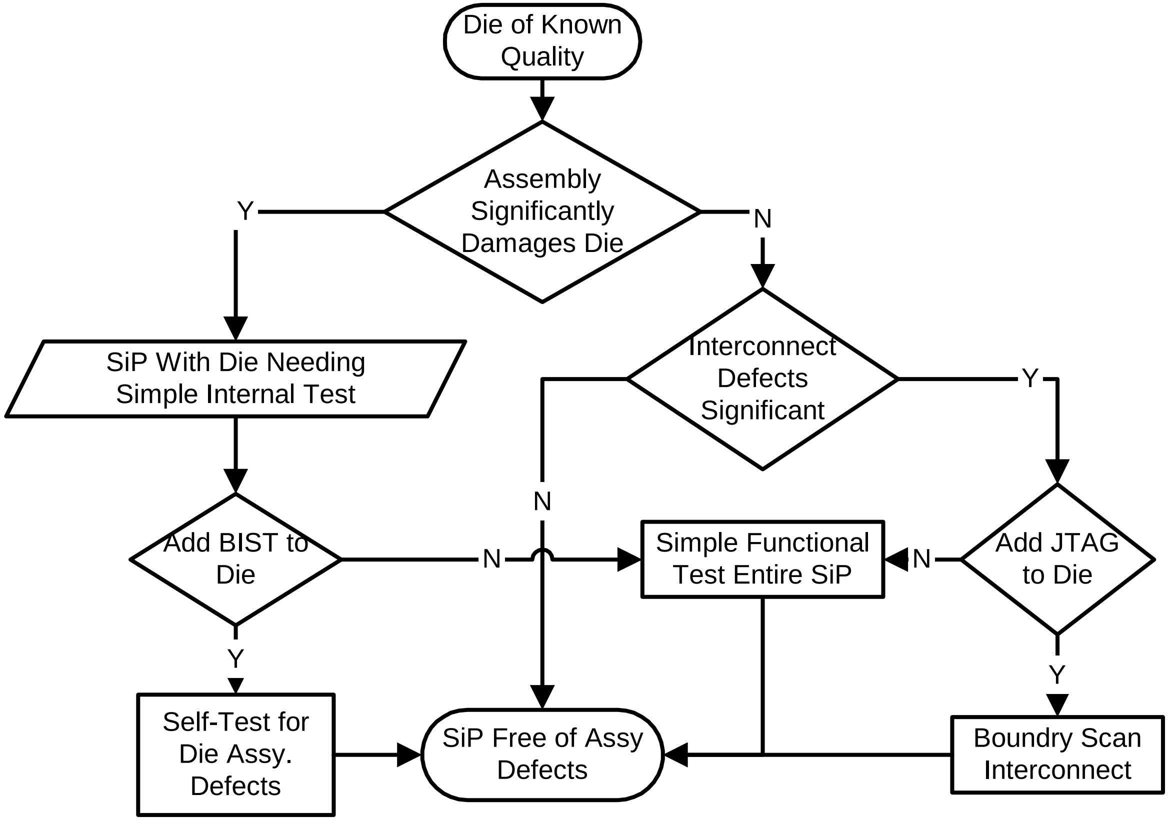
Packaged Die Needing No Further Internal Testing

Assemble & Test Die Sequentially

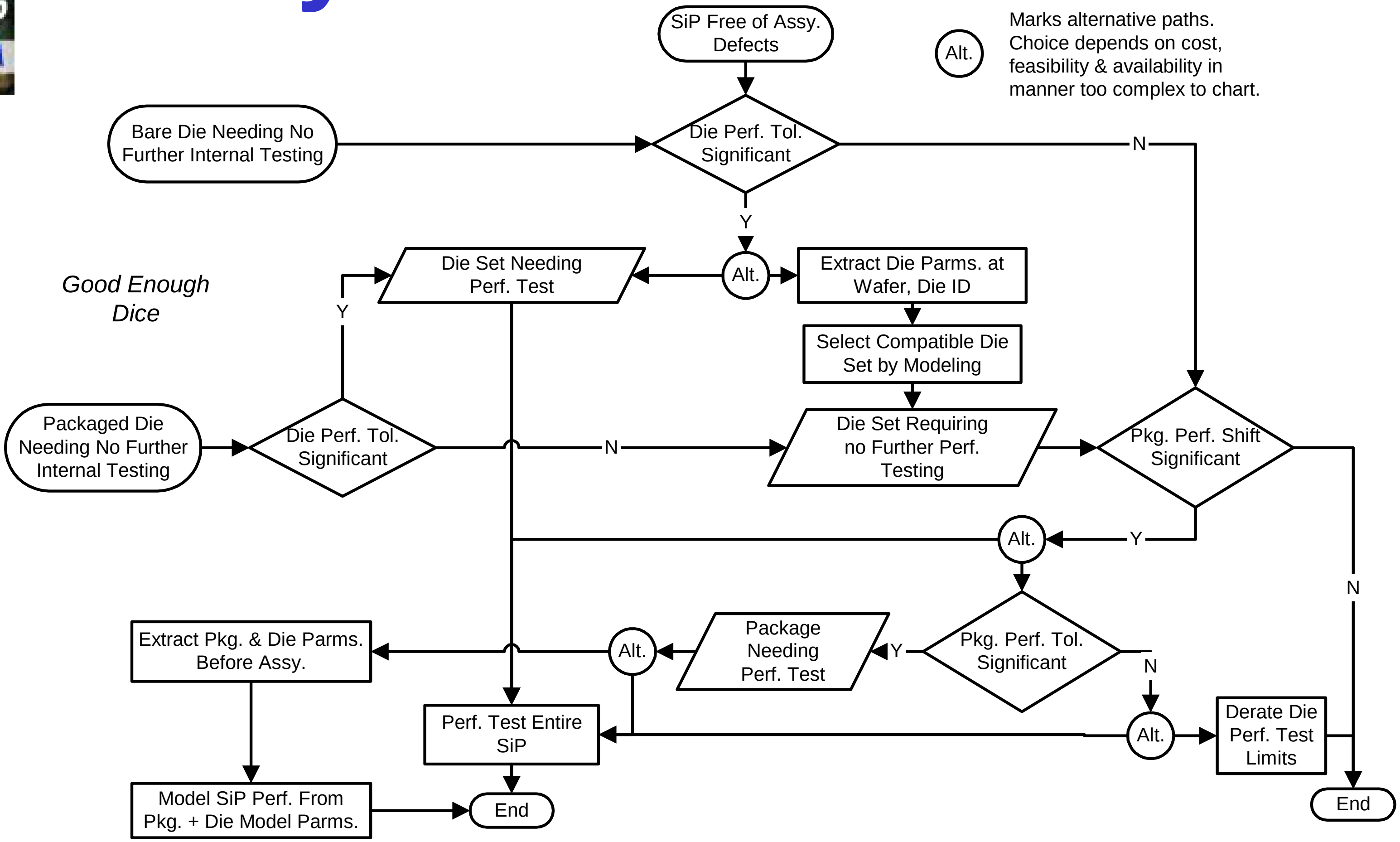
Package Test Die in Multiple Insertions

Assembly Defects

- Does assembly process damage die?
- Die defects usually not separated from pkg. interconnect defects
- Interconnect defects can be found with simple boundary scan “board” test
- Can BIST find the few assembly-induced die defects?


Die of Known Quality
Assembly Significantly Damages Die
Y
N
SiP With Die Needing Simple Internal Test
Interconnect Defects Significant
Y
N
Add BIST to Die
N
Y
Simple Functional Test Entire SiP
N
Add JTAG to Die
Y
Self-Test for Die Assy. Defects
SiP Free of Assy Defects
Boundry Scan Interconnect

System Tolerances



SiP Free of Assy. Defects

Alt. — Marks alternative paths. Choice depends on cost, feasibility & availability in manner too complex to chart.

Bare Die Needing No Further Internal Testing

Die Perf. Tol. Significant

N

Y

Good Enough Dice

Die Set Needing Perf. Test

Alt.

Extract Die Parms. at Wafer, Die ID

Select Compatible Die Set by Modeling

Y

Packaged Die Needing No Further Internal Testing

Die Perf. Tol. Significant

N

Die Set Requiring no Further Perf. Testing

Pkg. Perf. Shift Significant

Alt.

Y

N

Extract Pkg. & Die Parms. Before Assy.

Alt.

Package Needing Perf. Test

Y

Pkg. Perf. Tol. Significant

N

Perf. Test Entire SiP

Alt.

Derate Die Perf. Test Limits

Model SiP Perf. From Pkg. + Die Model Parms.

End

End

- Defect-free dice & pkg. may not build working system because of tolerance accumulation
- If all components performance tested, system can be verified by simulation rather than measurement
- Even select components to max. yield or perf. by simulation
- Perf. test of SiP only needed when package performance tolerance significant

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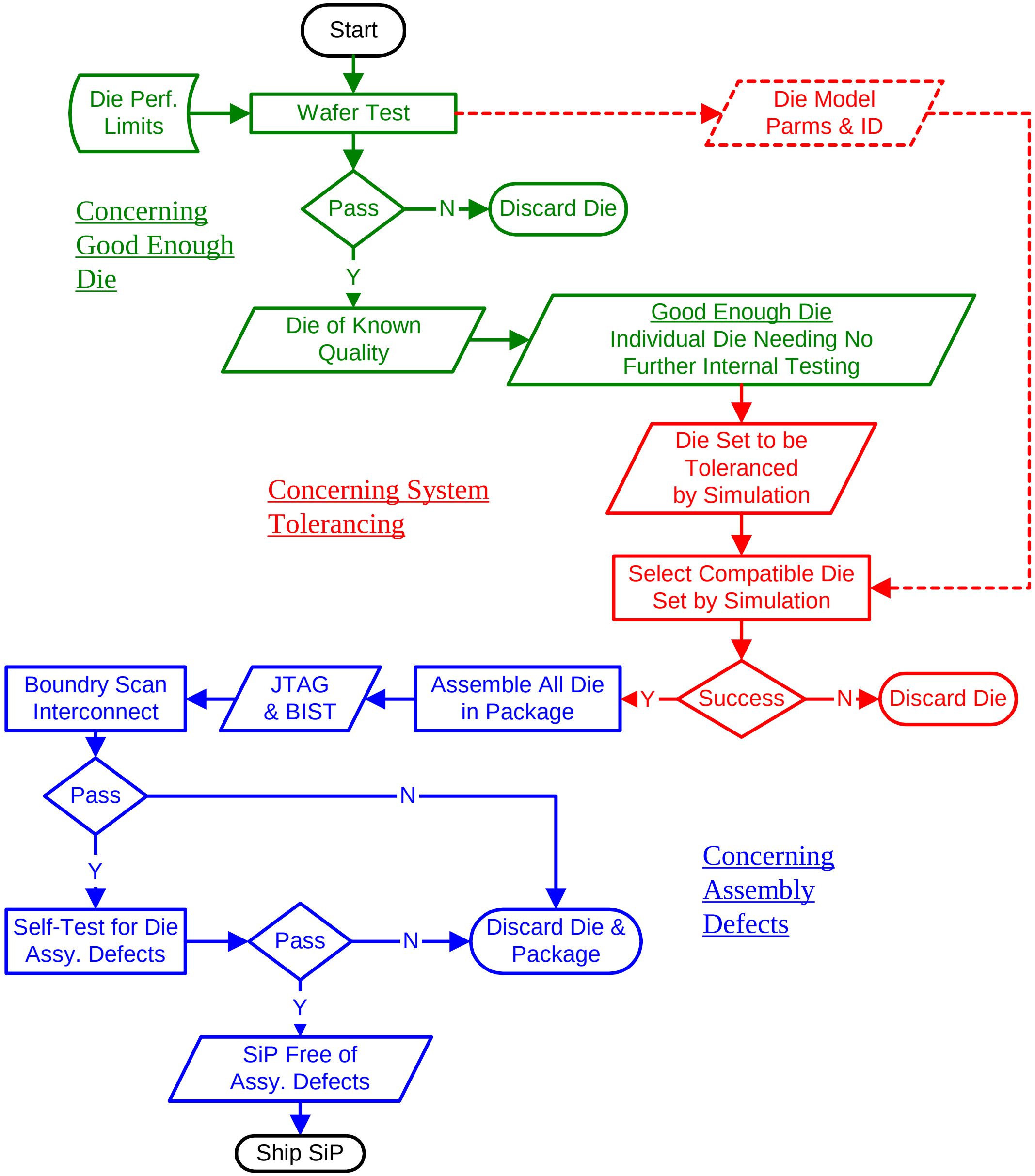
An Optimum Test Flow

- An intelligent set of test choices
- Can’t work for every design
- Make wafer test good enough no further die internal testing needed – Good enough KQD
- Pass results to simulator for die tolerancing/optimization
- Package performance tolerance insignificant
- Assembly only introduces interconnect defect that are boundary scan tested
- *Is outgoing quality high enough w/o final performance test?*



Conclusions

- Quality requirements & test effort are not absolutes – Replace by modeling of quality vs. cost for the specific product & mfg. process
- Replace concept of KGD with KQD, assumption with knowledge
- Use knowledge of parts & process to design test flow to only screen (to required level) defects created by preceding operation or haven't been adequately screened earlier
- Communicate up & down mfg. chain to maximize use of information collected, i.e. replace redundant tests with simulations