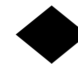
2005 Packaging Roadmap Overview



Sept 12, 2005

Joe Adam Skyworks

Major Packaging Industry Trends

- Volume drivers have shifted to consumer electronics
- Longer term growth will be driven by machine to machine
- System In Package has become a mainstream technology
- Chip Scale Packages are beginning to replace older leadframe technologies due to cost, size, and performance advantages
- Wafer level packaging technologies is taking off
- The contract assembly and test business has started to consolidate driven by a more competitive environment
- The EMS and Assembly and Test overlaps are increasing
- Improvements in cost are not keeping pace with pricing pressure

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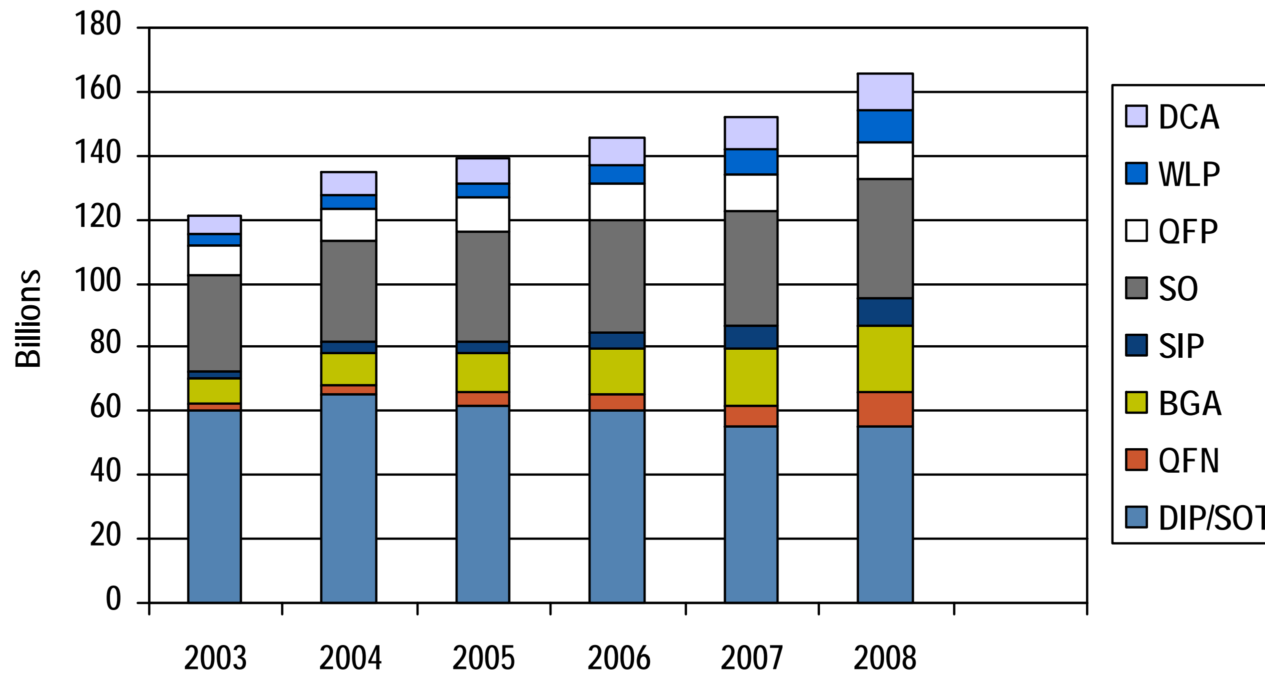
Shifts In Packaging Technology



Source: Electronic Trends Publications and Prismark

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Industry Challenges in the Next Five Years

- Tools and methodologies to address chip and package co-design
  - Mixed signal co-design and simulation (SI, Power, EMI)
  - For transient and localized hot spots - simulation of thermal mechanical stresses, thermal performance and current density in solder bumps
- Close the Gap between chip and substrate interconnect density
  - Increased wireability and dimensional control at low cost
  - Higher temperature stability and lower moisture absorption
  - TCE and Modulas better matched to low K flip chip requirements
- Wafer Level Packaging
  - I/O pitch between 250um 400um less than 100 I/O
  - Solder joint reliability and cleaning processes for low stand-off
  - Wafer thinning and handling technologies
  - Compact ESD structures
- Impact of Cu/low k on Packaging
  - Direct wire bond and UBM/bump to Cu to reduce cost
  - Lower TCE and modulus substrates to reduce die level stress in flip chip
  - Lower strength in low k which creates a weaker mechanical structure

Package Technology Requirements

Year of Production	2004	2005	2006	2007	2008	2009
Cost per Pin Minimum for Contract Assembly [1,2] (Cents/Pin)						
Low-cost, hand-held and memory	0.30–.53	.27–.50	.26–.48	.25–.45	.23–.43	.22–.41
Cost-performance	.71–1.24	.67–1.17	.64–1.11	.61–1.05	.58–1.00	.55–.96
High-performance	1.88	1.78	1.69	1.61	1.52	1.45
Harsh	0.32–2.88	0.29–2.60	0.26–2.33	0.25–2.11	0.23–2.00	0.22–1.90
Chip Size (mm^2) [3]						
Low-cost	100	100	100	100	100	100
Cost-performance	140	140	140	140	140	140
High-performance	310	310	310	310	310	310
Harsh	100	100	100	100	100	100
Maximum Power ($Watts/mm^2$) [4]						
Low-cost (Watts) [5]	2.7	2.8	3	3	3	3
Cost-performance	0.6	0.65	0.7	0.74	0.79	0.83
High-performance	0.51	0.54	0.58	0.61	0.64	0.64
Harsh	0.16	0.16	0.18	0.18	0.2	0.2
Package Pincount Maximum [6][7]						
Low-cost	122–500	134–550	144–600	160–660	180–720	180–800
Cost-performance	500–1600	550–1760	550–1936	600–2140	600–2400	660–2800
High-performance	3000	3400	3800	4000	4400	4600
Harsh	500	550	600	660	720	780

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Package Technology Requirements

Minimum Overall Package Profile (mm)	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*
Low-cost	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Cost-performance	**0.8**	**0.8**	**0.8**	**0.8**	**0.65**	**0.65**
High-performance	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**	**N/A**
Harsh	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**
Performance: On-Chip (MHz)[8]						
Low-cost	**552/5200**	**607/3865**	**668/4251**	**735/4676**	**800/5000**	**830/5150**
Cost-performance	**3990**	**5170**	**5630**	**6740**	**—**	**—**
High-performance	**3990**	**5170**	**5630**	**6740**	**—**	**—**
Harsh	**80**	**88**	**96**	**106**	**116.6**	**128.26**
Performance: Chip-to-Board for Peripheral Buses (MHz) [9]						
Low-cost	**100**	**100**	**100**	**100**	**100**	**100**
Cost-performance (for multi-drop nets)	**533**	**600**	**667**	**733**	**800**	**800**
High-performance (for differential-pair point-to-point nets)	**2500**	**3125**	**3906**	**4883**	**6103**	**7629**
Harsh	**80**	**88**	**96**	**106**	**106**	**115**

CONNECT WITH AND STRENGTHEN YOUR SUPPLY CHAIN

Die to Package Interconnect Requirements

Year of Production	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Wire bond pitch - ball	**40**	**35**	**35**	**30**	**30**	**25**	**25**	**25**	**25**	**25**	**25**	**25**
Wire bond pitch -wedge	**30**	**30**	**25**	**20**	**25**	**20**	**20**	**20**	**20**	**20**	**20**	**20**
TAB	**35**	**30**	**30**	**25**	**25**	**25**	**20**	**20**	**20**	**15**	**15**	**15**
Flip chip area array*	**150**	**130**	**130**	**120**	**110**	**100**	**90**	**90**	**90**	**80**	**80**	**70**
Peripheral flip chip Stud Bump	**60**	**40**	**40**	**30**	**30**	**20**	**20**	**20**	**20**	**15**	**15**	**15**

Note: Validation for 100 um pitch required

Package I/O Pitches

BGA Solder Ball Pitch (mm)	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Low-cost and hand-held	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
Cost-performance	0.8	0.65	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
High-performance	1	1	0.8	0.8	0.8	0.8	0.65	0.65	0.5	0.5	0.5	0.5
Harsh	0.8	0.8	0.8	0.65	0.65	0.65	0.65	0.5	0.5	0.5	0.5	0.5
Chip Scale Package Pitch	0.4	0.3	0.3	0.2	0.2	0.2	0.2	0.15	0.15	0.15	0.1	0.1

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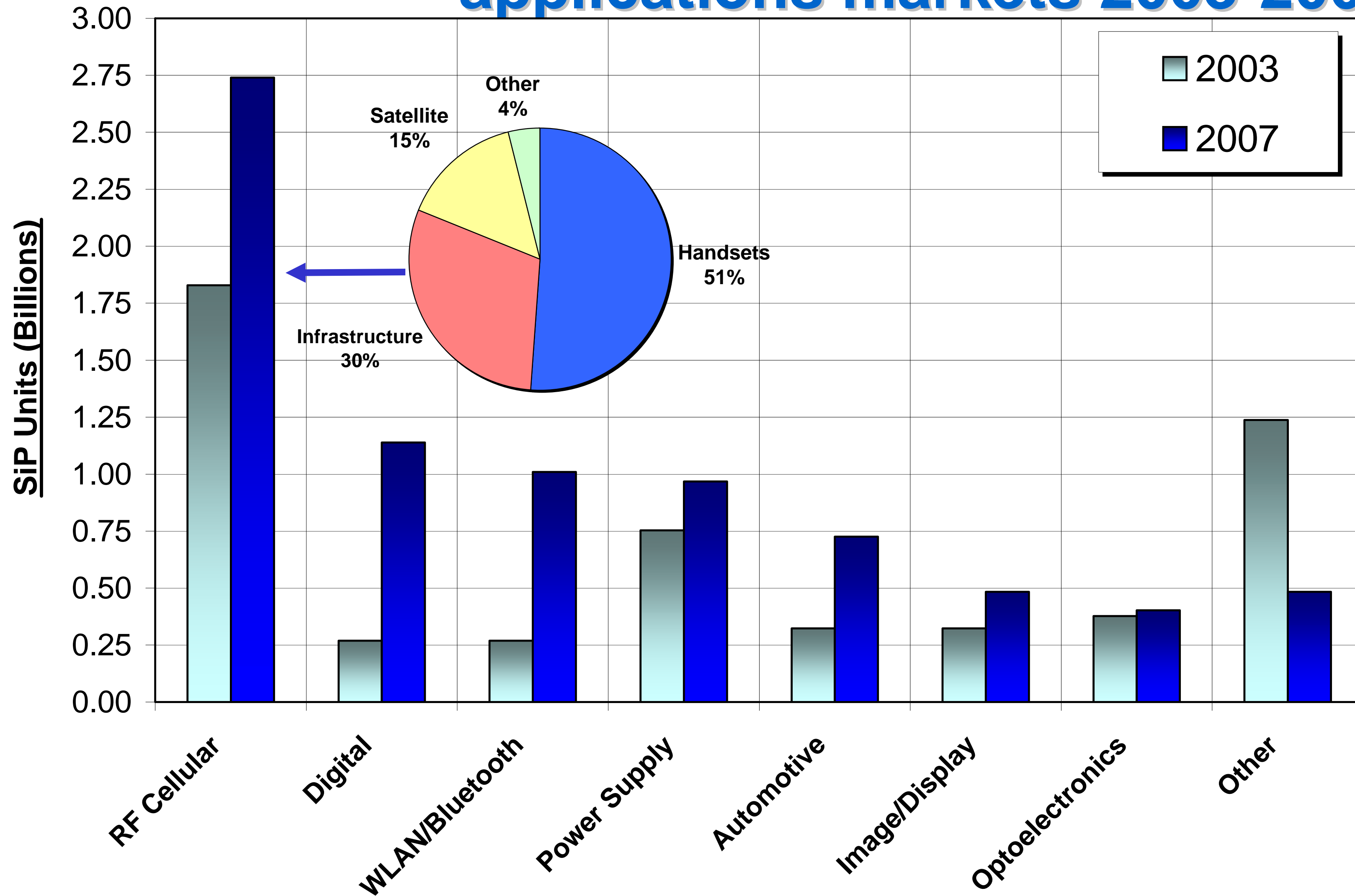
Projected growth for SiP in key applications markets 2003-2007



Sources: Prismark.

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System In Package Roadmap

System In Package Requirements												
Year of Production	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2012*	*2013*	*2015*	*2016*	*2018*
Digital networks- max I/O	*2600*	*2900*	*3000*	*3200*	*3500*	*3500*	*3500*	*3500*	*3500*	*3500*	*3500*	*3500*
RF products - max I/O	*150*	*200*	*200*	*200*	*200*	*200*	*200*	*200*	*200*	*200*	*200*	*200*
Max number of stack die	6	7	8	8	8	8	8	8	8	8	8	8
Max number die in Module	10	12	12	12	12	12	12	12	12	12	12	12
Minimum Component size in.	0201	0201	01005	01005	01005	01005	01005	01005	01005	01005	01005	01005
Die Pad pitch - wirebond	40	35	35	30	30	25	25	25	25	25	25	25
Die pad pitch - flipchip	150	130	130	120	110	100	90	90	80	80	70	70
Embedded Passives in Laminate	L	L	CL	CL	CL	CL	CL	CL	CL	CL	CL	CL
Embedded Passives in Ceramic	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C	R, L, C
MSL Level	2a	2	2	2	2	2	2	2	2	2	2	2
Mx Reflow temp C	260	260	260	260	260	260	260	260	260	260	260	260

Conclusions

- The industry growth will be driven by consumer and machine to machine based applications going forward
- SIP and WLP technologies will be a key element of this growth and are shifting the industry research focus
- To improve R&D return and effectiveness the industry needs to increase collaboration through partnerships and shared R&D
- Emerging devices will required a new set of packaging technologies that allow devices to interact with the environment instead of being protected from it