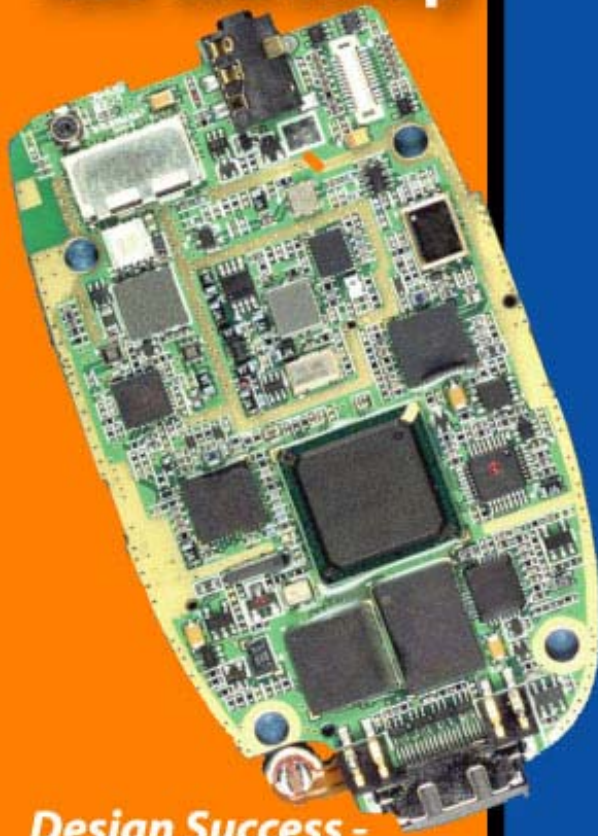


12th Annual

KGD

**Packaging &
Test Workshop**



*Design Success -
KGD Starts
at the Beginning*

Sept. 11-14, 2005 , Napa, CA

Built-in-Test Solutions for SiP

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Outline

❖ Introduction

- *Motivation*
- *Converters: types of errors & parameters*

❖ Estimation and compensation techniques

- *Stochastic errors*
- *Non-linearities*

❖ Application to SiP

- *Loop-back*
- *Test methodology*

❖ Conclusions / Further works

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Motivation

“SiP final test requires a greater **diversity** of ATE resources than SoC. It also leads to large **disparities** in test times and resource utilization among die” (P. O’Neill, Agilent Technologies)



Solutions:

- ✓ Insert in multiple testers = **long test time, complex flow**
- ✓ ‘Intelligent’ scheduling of test resources to allow parallel test of each chip in SiP = **expensive ATEs**
- ✓ BIST = **DfT, DSP**

Motivation

So, we want **BIST!**

But, before BIST, let's start with **BIT** (Built-in-Test) solutions.

Our approach is:

1) Find methods using **DSP** (digital signal processing), because digital is easy to simulate, portable, reliable,..., and a low-cost tester is a digital one!

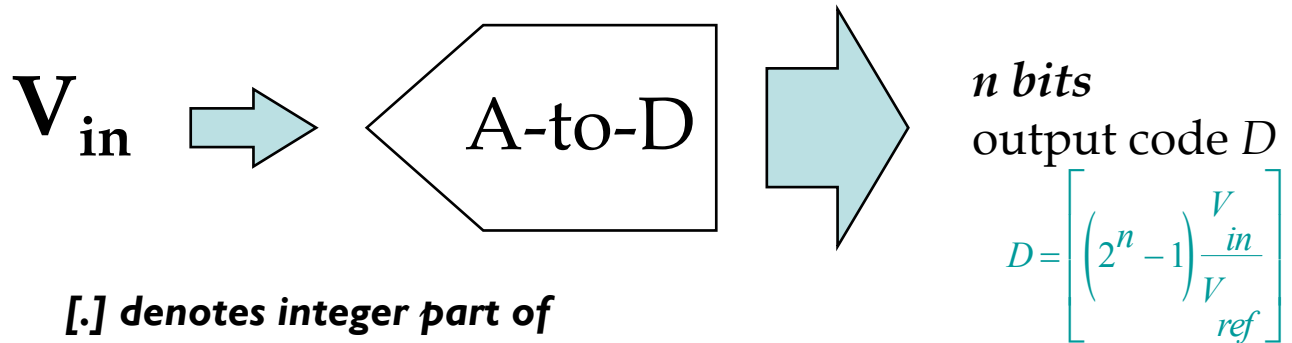
2) Find **DfT** (Design-for-Test) solutions to implement the methods

Then,

3) Introduce the **Self-Test** engines...

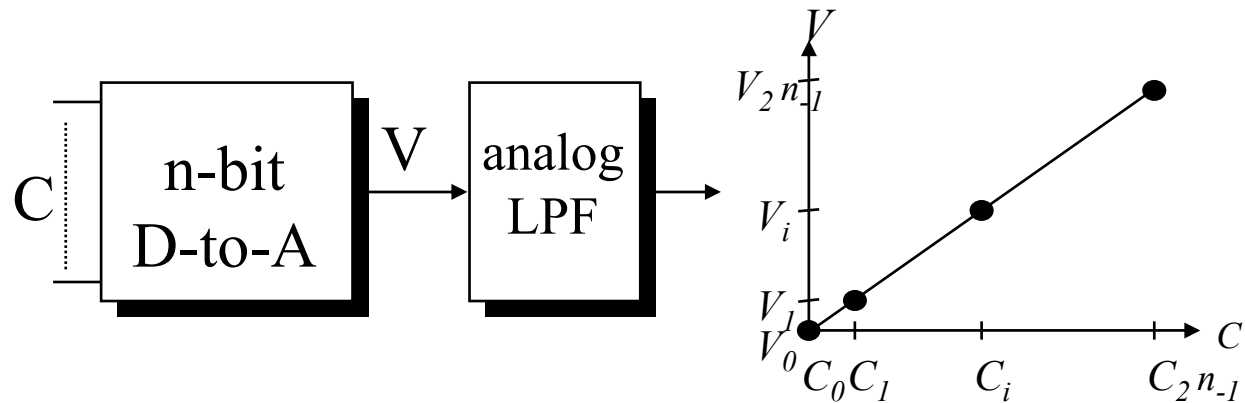
... starting with data converters, the path between analog and digital domains

Converters errors

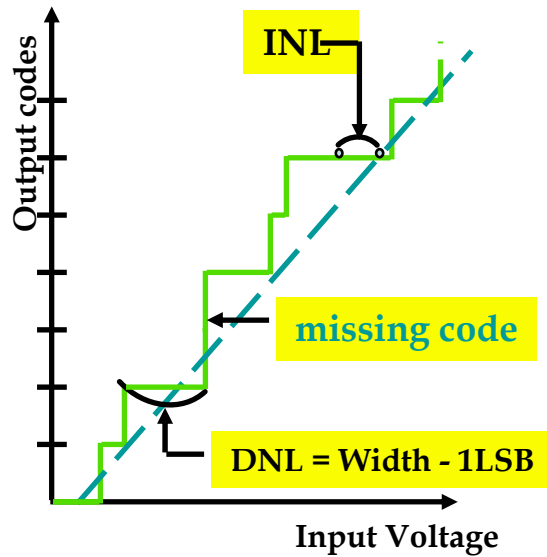


[.] denotes integer part of
 V_{ref} = input full-scale voltage

Conversion operation = sampling, quantization & encoding

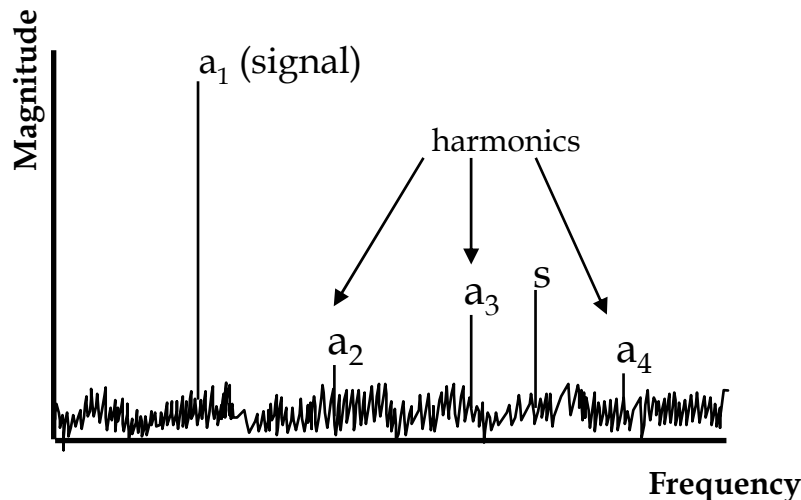


Converters errors



$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S}$$

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S} - 1$$



$$THD[dB] = 10 \log \frac{P_{harmonics}}{P_{signal}}$$

$$SNR[dB] = 10 \log \frac{P_{signal}}{P_{noise}}$$

Converters errors

- The errors generated by a Data Converter may be split into 2 categories:
 - Stochastic: noise (thermal effect, mainly) + jitter (clock phase noise, mainly)
 - Deterministic: INL => distortion
- These errors are **masked by the ATE** ones, so test becomes more and more inaccurate wrt converters performances
- Question: how to **estimate and compensate** the ATE errors:
 - At max speed, and
 - Using a reduced sample set?

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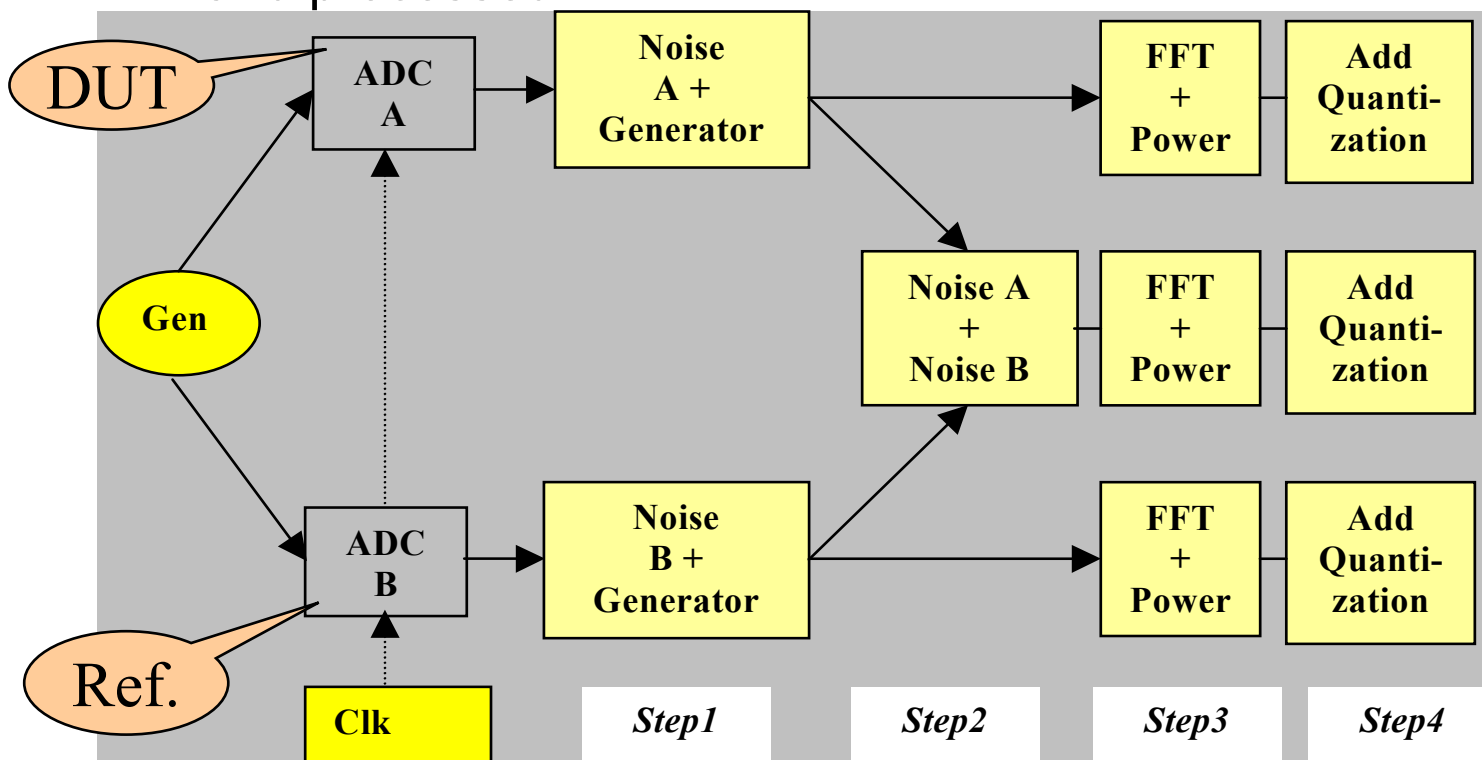
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Jitter + noise compensation

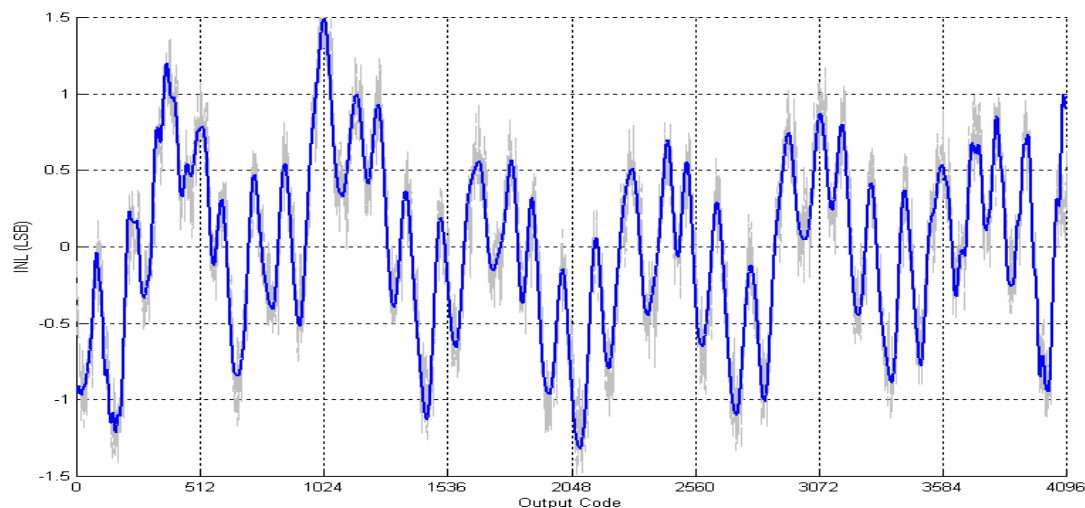
- Noise is considered as a random variable
Correlated and uncorrelated values are discriminated and processed



Ref: "Improving the dynamic measurement of ADC's using the 2 ADC method"
P Cauvet, Teradyne Users Group 2001

INL estimation

- INL is commonly estimated using the **Histogram Method**, requiring typically: 2M samples for a 12-bit converter
- A novel method, based on **Spectral Analysis**, makes use of 8k samples only!



Ref: "Estimation of A/D Converter Nonlinearities from complex Spectrum",
J.M. Janik, Proc. IWADC Modeling and Testing, pp.8-10. September 2003

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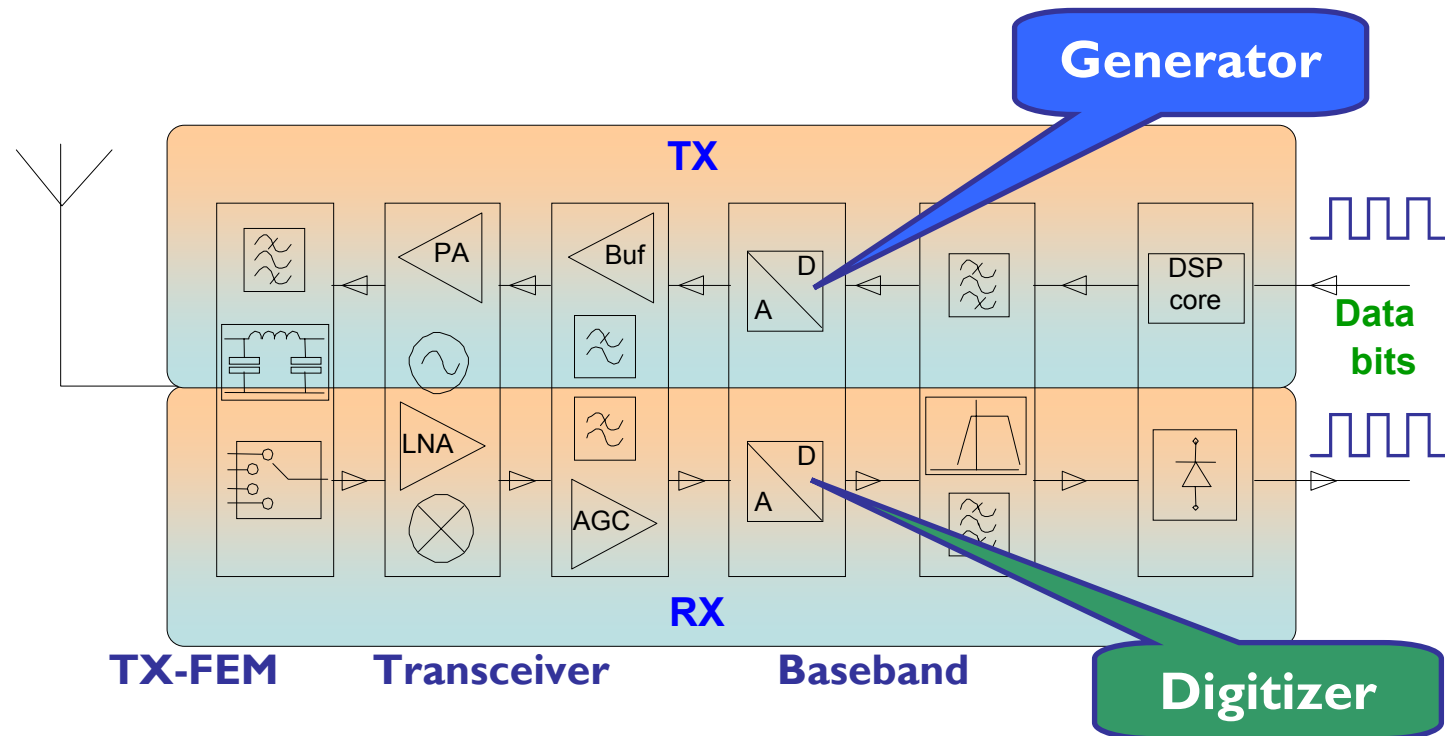
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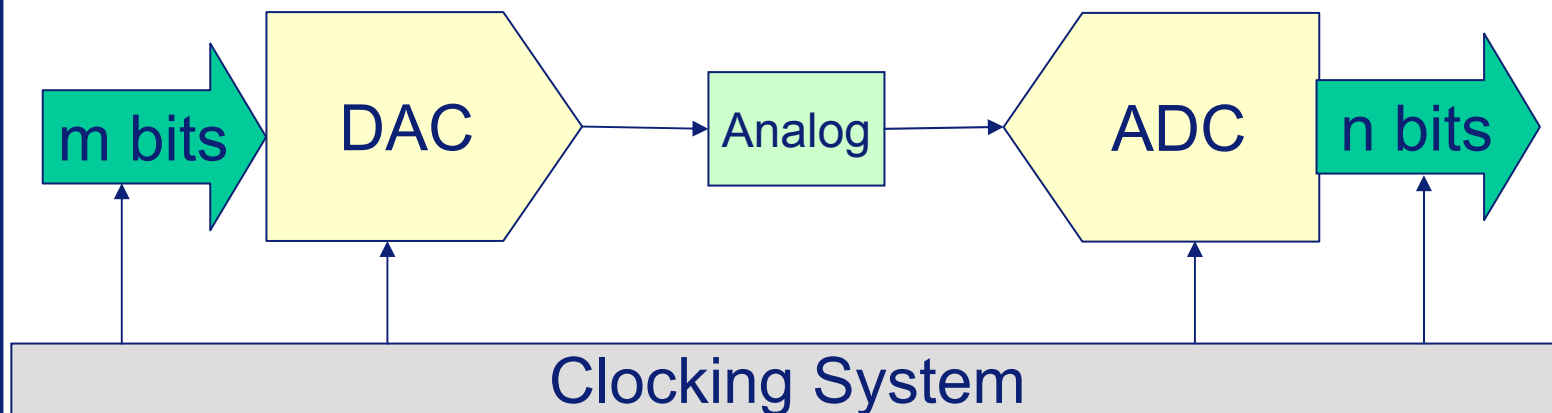
Application to SiP

- Converters are present in most of the SiPs
- Idea: re-use them for tests and diagnostics, as embedded instruments

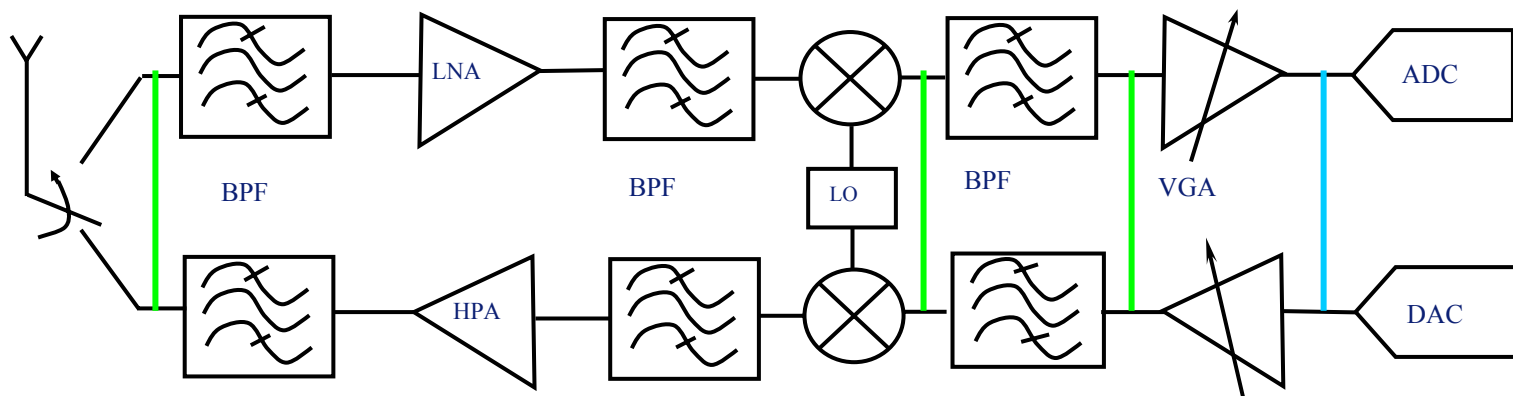


Application to SiP

- **Objective:**
 - Develop DSP solutions to get rid of expensive tester options. Then, convert them into BIST solutions for auto-test.



Loop-back

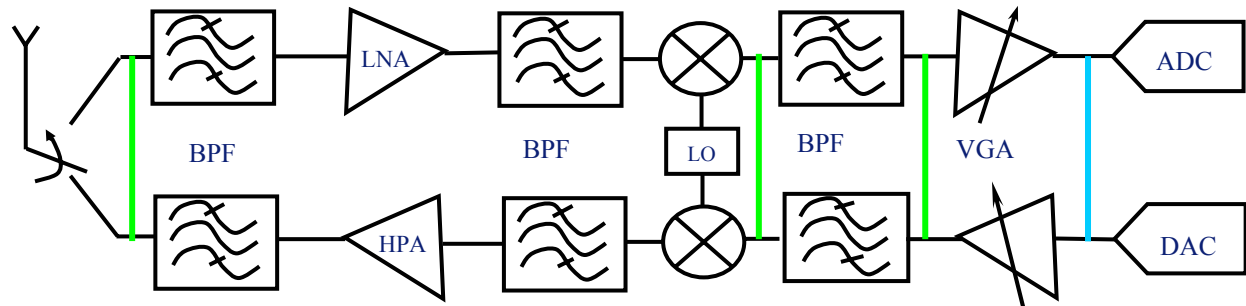


Architecture transceiver RF + converters

Ultimate goal: RF blocks will be tested using MS and Digital cores

- ADC ⇔ Digitizer
- DAC ⇔ Arbitrary Waveform Generator (AWG)

Loop-back



Advantages:

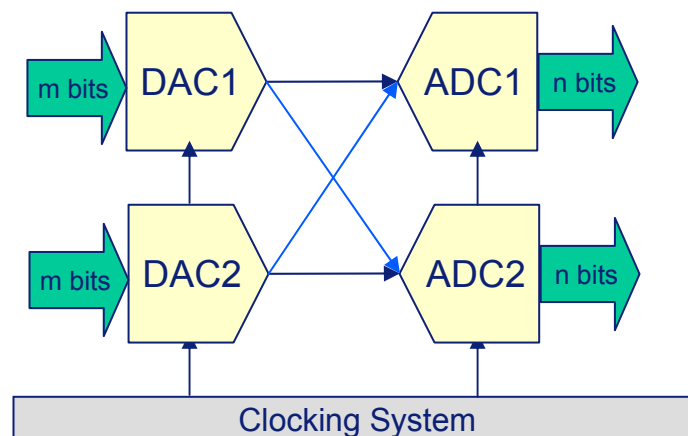
- ❑ No limitation in speed
- ❑ No external signals
- ❑ Reduction of tester resources

Issues:

- ❑ Resolution of converters: Fortunately, we can benefit from our previously developed techniques to “artificially” increase the resolution of the converters, so use them as instruments
- ❑ Handling internal signals (DfT)

Test Methodology

1. Capture **DAC1+ADC1** and **DAC2+ADC2**
2. Capture **DAC1+ADC2** and **DAC2+ADC1**
3. Capture other combinations

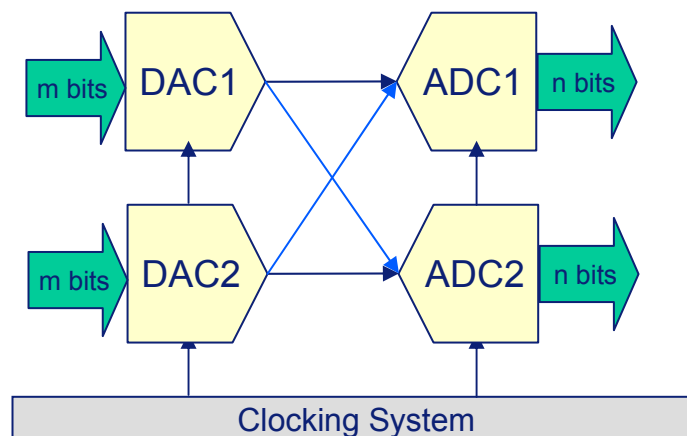


Then:

- Test
- Make diagnostics (in case of failure)
- Record the compensation parameters (when test passes)
- Activate the loop-back(s) and test the rest of the system

Test Methodology

1. *Noise and jitter can be estimated and compensated*
2. *Distortion is now partially estimated and compensated*



But:

- ❑ We need 2 DACs and 2 ADCs (not a big issue, in many cases)
- ❑ We need to carefully handle the analog signals (design issue)

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Conclusions / Further Works

- ❖ **DSP:** solutions are
 - *Available for stochastic errors compensation*
 - *Partly available for systematic errors*

- ❖ **DfT:** next step towards a BIST solution
 - *Some solutions are already available*
 - *They are dedicated to the type of application*
 - *Needs for changing the test methodology?*

Thank you

Questions?