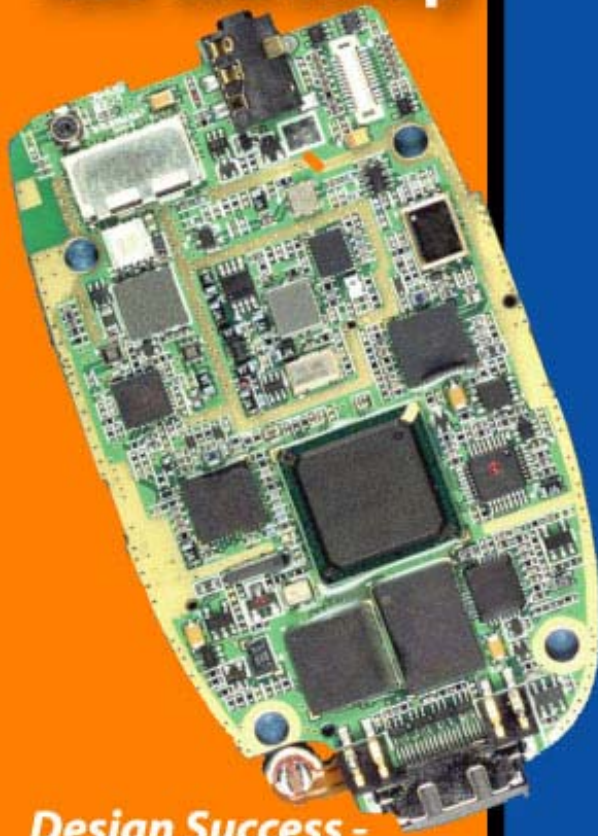


12th Annual

**KGD**

**Packaging &  
Test Workshop**



*Design Success -  
KGD Starts  
at the Beginning*

Sept. 11-14, 2005 , Napa, CA

# **Known-Good-Die Test Strategies**

Anton Chichkov  
Test Meth Eng Manager  
AMIS

# Summary

- KGD Test Challenges
- KGD Test Methods
  - Over-voltage stress
  - Timing Related Faults Testing
  - Current based test methods
  - Min Vdd testing
  - Analogue blocks testing
  - SPP
    - SPAT/DPAT
- Mixed Signal Testing for <10 PPM

# KGD Test Challenges

- Delivering product that meets the quality expectations
  - In areas like automotive, medical, and in types of products employing KGD these requirements are in ranges 50, 10, 0 PPM
- To meet needed quality levels within the expectation of human and capital investments

# KGD Challenges

- New defect types appearing in the new technology nodes, requiring new test methodologies
- Yield learning is just beginning to show its potential
- The application of delay fault test methodology not yet fully matured
- Iddq test method is approaching its limits. Replacements must be found

# Test Methods

- Pre DSM standard
  - Stuck at fault testing
  - Current-based testing
  - Testing under different conditions (T,V)
- DSM methods
  - Transition fault
  - Low voltage testing
  - Combination of measured parameters

# Over-voltage stress

- Definition
  - Nondestructive supply voltage bigger than  $V_{dd\_max}$  is applied for limited time
    - Defect and Reliability oriented
    - The over-voltage introduces an acceleration of the fatigue provoked by defects resulting in failures on the ATE
- Dynamic
- Static

# Over-voltage stress

- Screening
  - V screen comparing during stress
  - V stress using other tests to screen
    - Structural and functional tests
    - Current based tests
    - Iddq before and after

# Over-voltage stress

- Effectiveness
  - Good for: Metal slivers, cracks in insulation layers and metal particles and residues, including metal particles with native oxide coating
  - Not so good for: opens, high resistive via
- Involved problems
  - Incorrect  $V_{stress}$  can cause yield loss due to overstress
  - In some cases  $V_{stress}$  can temporary cure the defect leading to test escapes

# Over-voltage stress

- Overlap with other techniques
  - V stress overlap significantly with burn in
    - Combination of good coverage Vstress and efficient Iddq is reasonably good replacement of BI
  - V stress overlap partially with Min\_Vdd

# Timing Related Faults Testing

- These techniques are addressing delay faults in static CMOS
  - Defect oriented
  - Existing SCAN structure is used to measure internal propagation delays or transient performance

# Timing Related Faults Testing

- Definition
  - ATPG targeting timing related faults. Mainly DFT challenge
- Path delay faults
- Transition faults
- Si Speed monitoring (on simple paths)
  - Si speed can be monitored for further combination with other methods like current based and min Vdd

# Timing Related Faults Testing

- Effectiveness
  - Any clock generation distribution design/process marginality
    - Duty cycle degradation in DLL/PLLs unbalanced clock trees ... ..
  - Faults associated with an increased resistance:
    - Incompletely filled via
    - Or mouse bites in interconnects
  - Faults associated with high resistive bridges in the data path

# Timing Related Faults Testing

- Involved problems
  - EDA tools are not completely mature
  - Requires manual intervention to ensure the quality of the test patterns. Especially for small delay faults
    - The amount of small delay fault is in the order of the amount of gross delay faults
    - Typical impact of these small delay faults is not sufficient to affect the performance of an IC. The large local current densities at these small defect location however makes them a reliability risk

# Timing Related Faults Testing

- Overlap with other techniques
  - Transitional or propagation delay testing significantly overlaps with Min Vdd. Advantage more deterministic coverage
  - Timing related methods have some overlap with Iddq/Vstress concerning mainly the category of high resistive bridging

# Current Based Testing

- Definition
  - Monitoring of CMOS static supply current
- Effectiveness
  - Very big coverage due to very good observability
  - Defect and Reliability oriented

# Current Based Testing

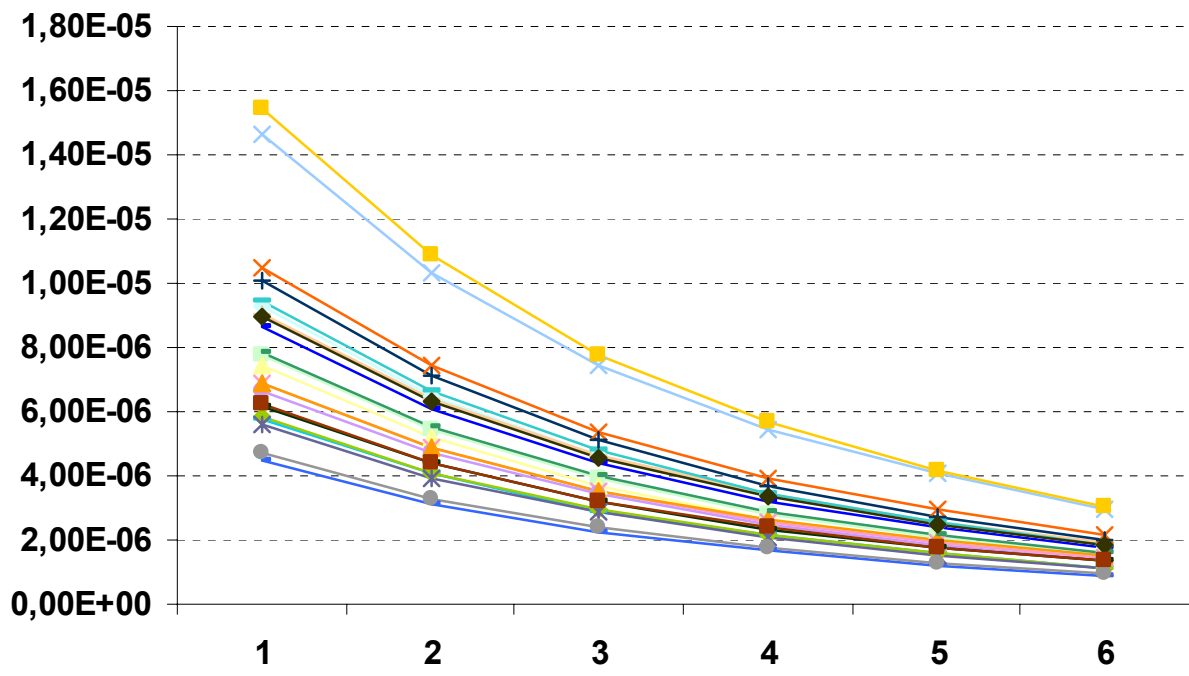
- Single limit Iddq
  - Run out of steam for the new DSM technologies
- Idd deltas and variations
  - Delta before and after stress
  - Delta over patterns
  - Delta over voltages
  - Iddq signature analyses
  - Iddt

# Multiple V Point Iddq

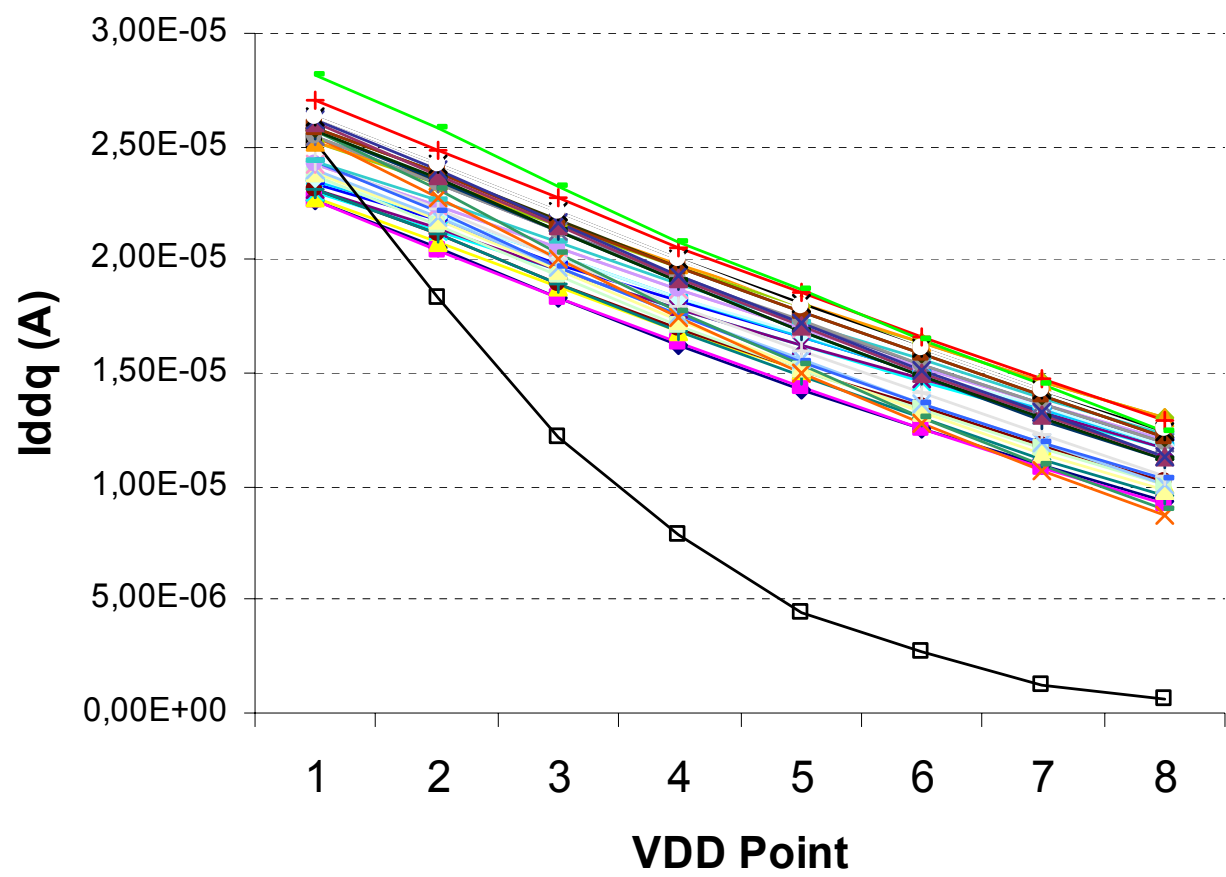
- Iddq is measured for several (5 - 7) different Vdds. Curve  $I = f(V)$  is build for every device and compared with golden curve
  - Good correlation with the results of other well established methods

# Multiple V Point Iddq

- Relation between good curves

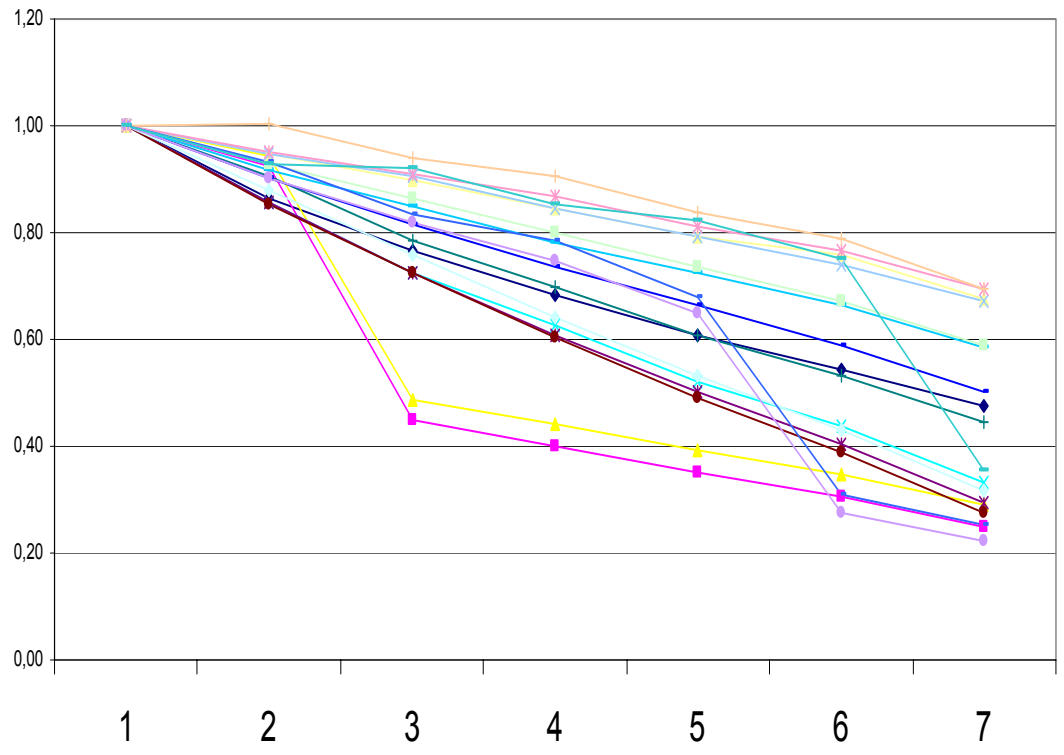


# Multiple V Point Iddq



# Multiple V Point Iddq

Iddq/I0  
bin8 and 11



# Min Vdd Testing

- Definition
  - Supply voltage lower than Vdd\_min where main population of dies is still functional
    - Defect and Reliability oriented
- Effectiveness
  - Metal shorts, Gate oxide shorts, Tunneling opens, Design/process marginalities, Temperature dependency

# Min Vdd Testing

- Involved problems
  - Limit definition is not so straight forward. Can cause hold situations in production due to excessive yield loss
- Overlap with other techniques
  - Min Vdd overlaps with timing related testing. And in certain degree with Iddq

# Analogue Test Methods

- DFT for mixed signal
  - Proper block isolation
  - Observability-controllability concerns
  - P1500 standard
- Spec based testing
  - Testing performance parameters of the circuit against test limits

# Analogue Test Methods

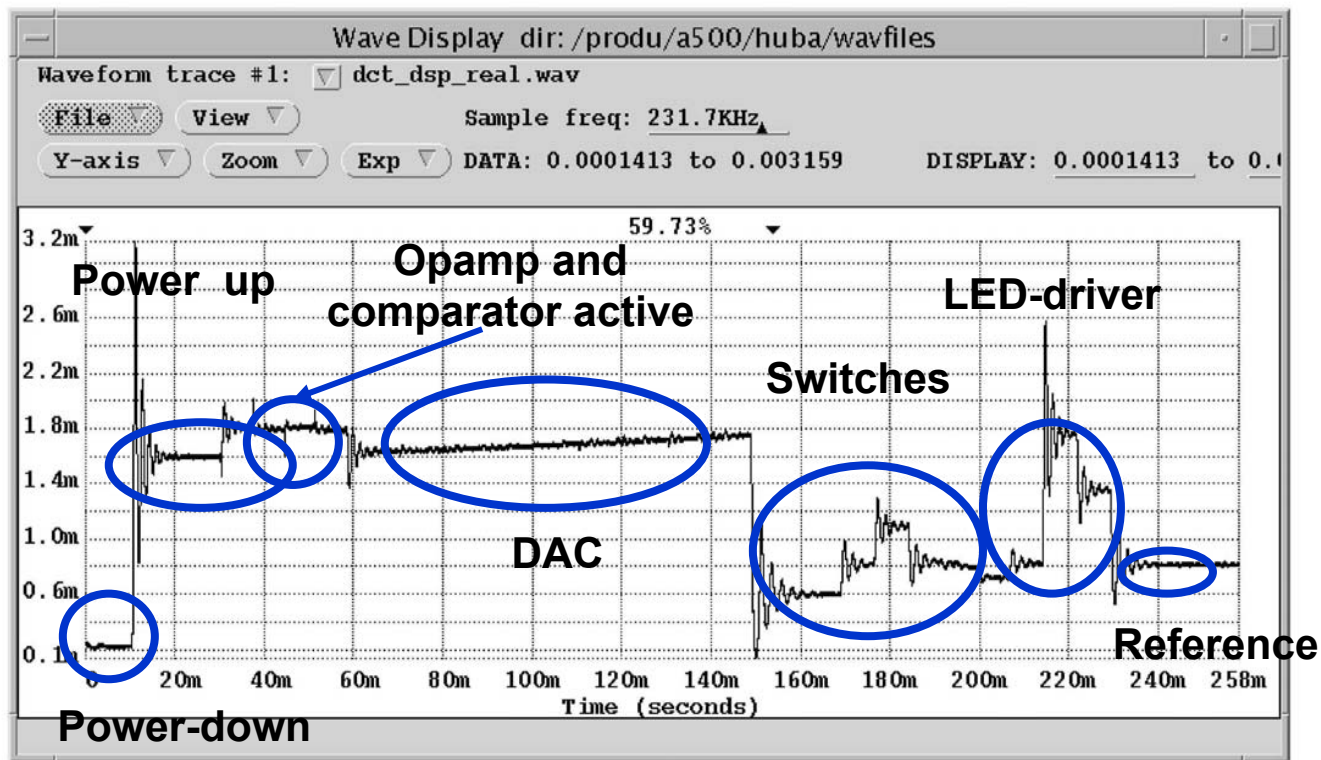
- Defect oriented testing
  - Oscillation Based Test
  - Impulse response signature testing
    - Impulse and step response tests
    - Sinusoidal oscillation tests
    - Cross-correlation methods
    - . . . . .

# Analogue Test Methods

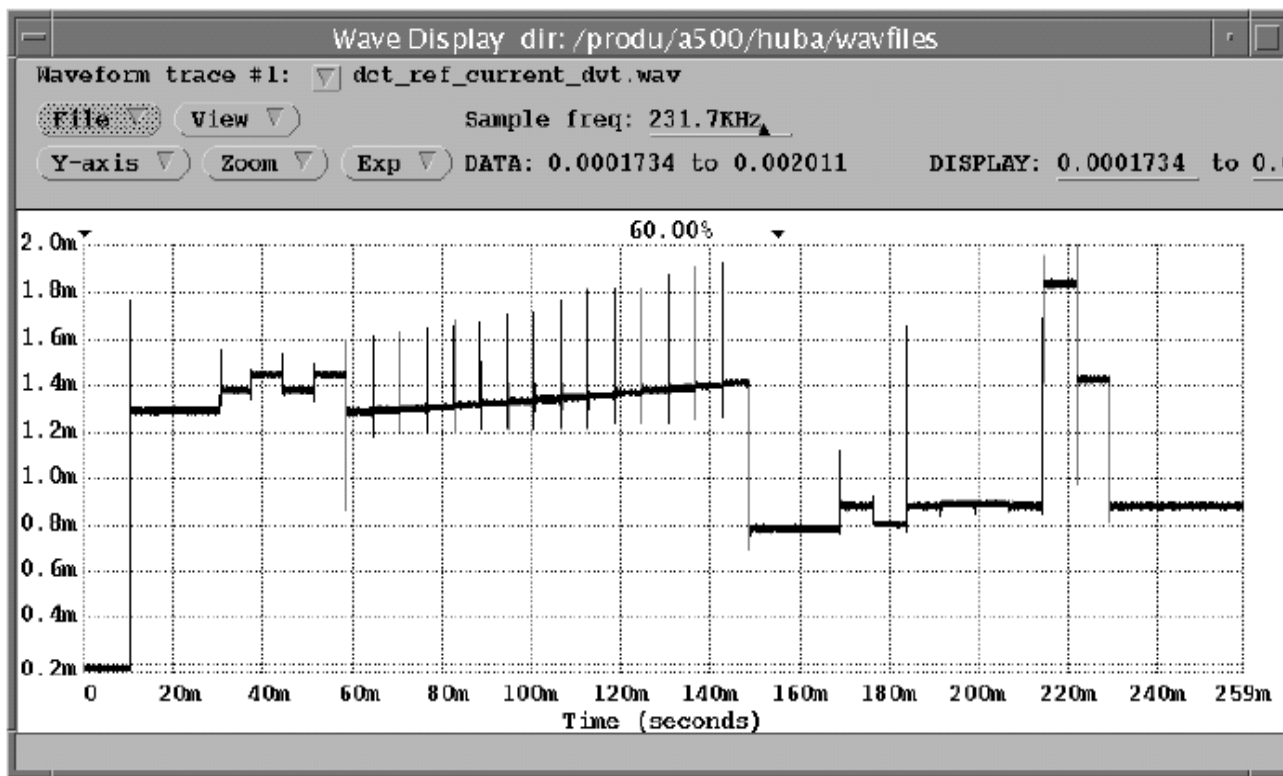
- ABIST
  - Signal generation on chip
  - Signal generation and data analyses on chip
  - Feed-Back Loop

# Analogue Test Methods

- Analogue supply current signatures



# Analogue Test Methods



Sept. 12-15, 2005

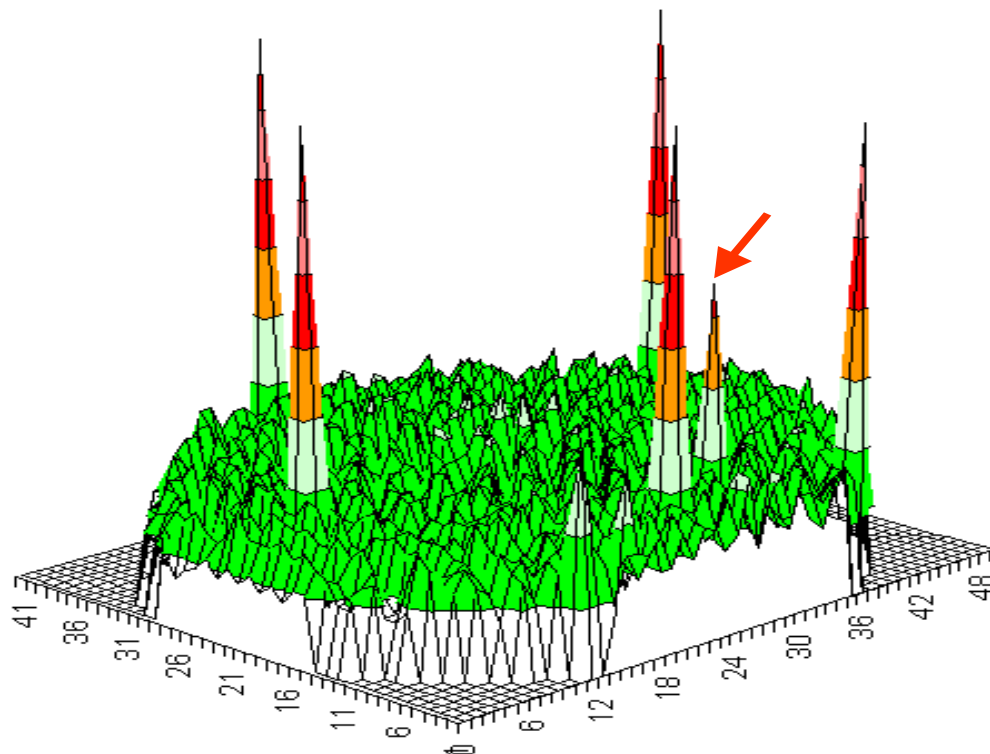
Napa, California

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# Statistical Post Processing Methods

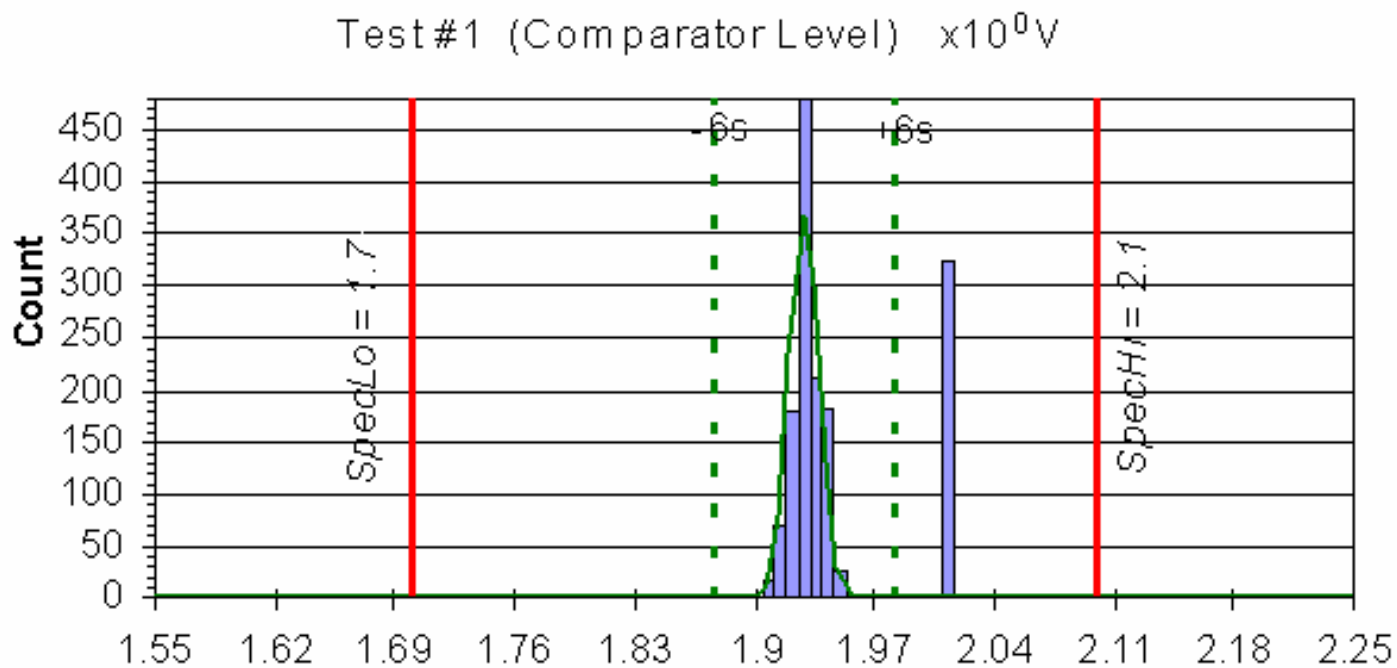
- Static/Dynamic Part Average Testing
  - Nearest Neighbor Residual
- Statistical Binning Analyses
- Device identification
  - Evaluation of reliability data in relation to yield and low yield events
  - Feed Forward Limits

# Part Average Testing



- **Diagram of the Voltage drop over a high-side driver across the wafer**

# Part Average Testing



- **Double distribution one standing just outside the calculated 6-sigma limit, leading to an unjustified yield loss**

# Testing For <10 PPM in Mixed Signal

- Coverage digital
  - ATPG as high as possible
  - Iddq 80% toggle rate
  - Memory 100% (BIST)
  - BIST and shadow circuitry testing
  - Vstress

# Testing For <10 PPM in Mixed Signal

- Coverage Analogue
  - Spec based testing 100% (per building block)
  - Analogue Vstress
  - Full path testing (for block interconnects)
  - Supply current testing

# Testing For <10 PPM in Mixed Signal

- Flow
  - Full characterization of packaged parts in the complete temperature range
  - Temperature wafer testing
  - Statistical Post processing
  - Coverage tuning based on customer data