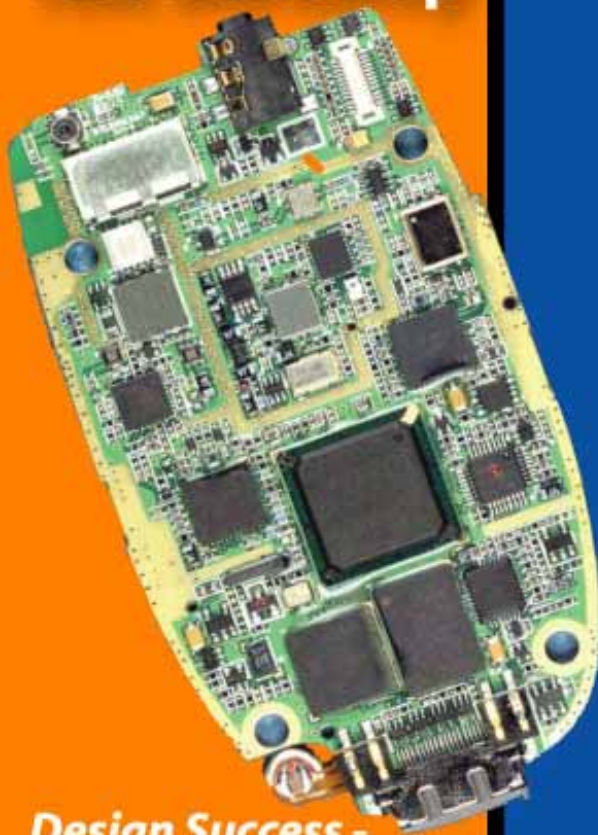


12th Annual

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**Packaging &
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*Design Success -
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Methodology to Skip the Memory Test Using ASB (At Speed Board)

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Contents

- What is ASB ?
- SiP type and needs
- Application of ASB in Memory test
- Future plan

What is ASB?

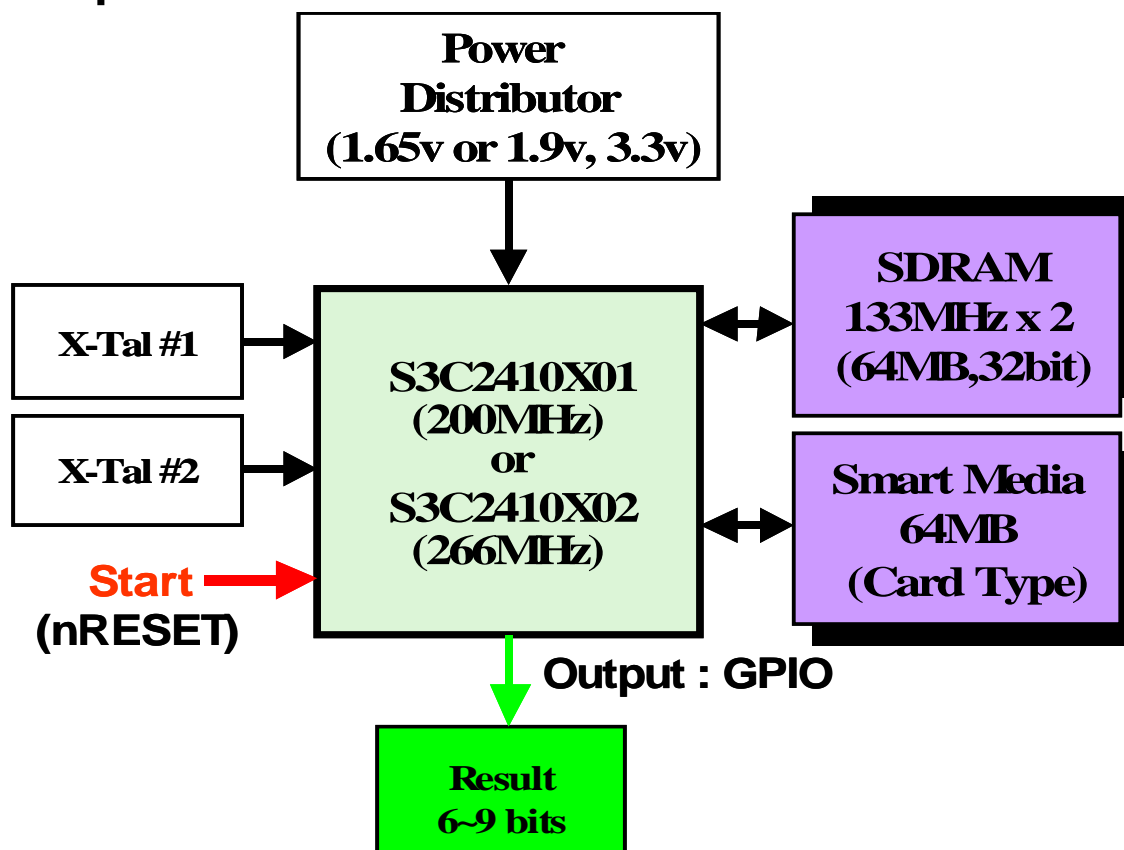
■ ASB (At Speed Board)

- Purpose
 - To guarantee the high speed operation
 - To skip ATE items
(Complicated and large vector items)
 - To guarantee the production capacity
(Parallel test)
 - To increase the fault coverage

What is ASB?

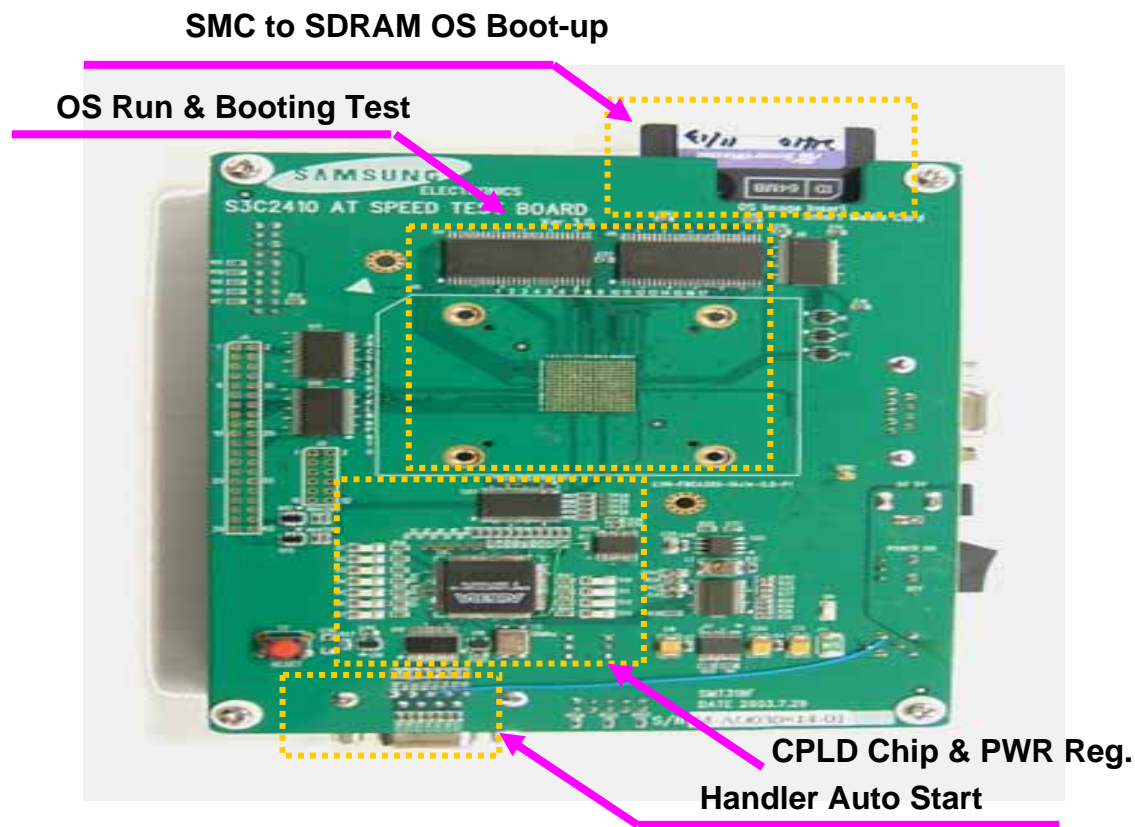
■ ASB (At Speed Board)

- Concept (Example)



What is ASB?

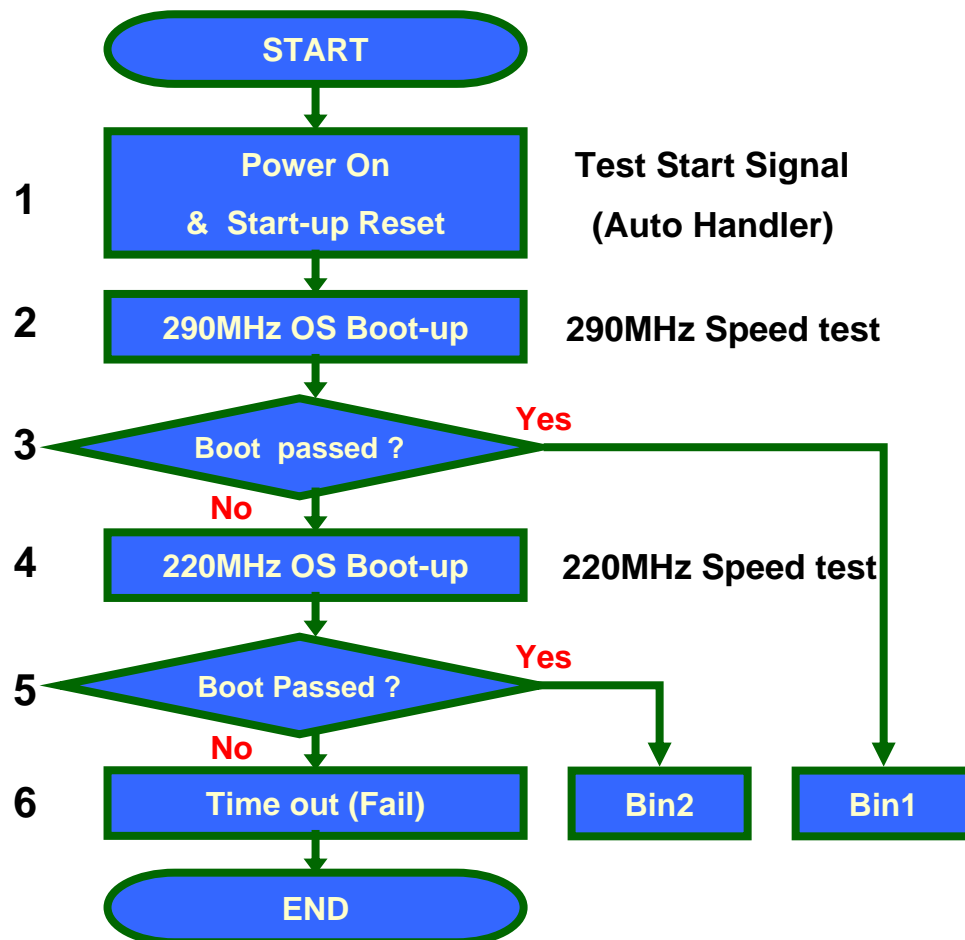
- ASB (At Speed Board)
 - Board configuration



What is ASB?

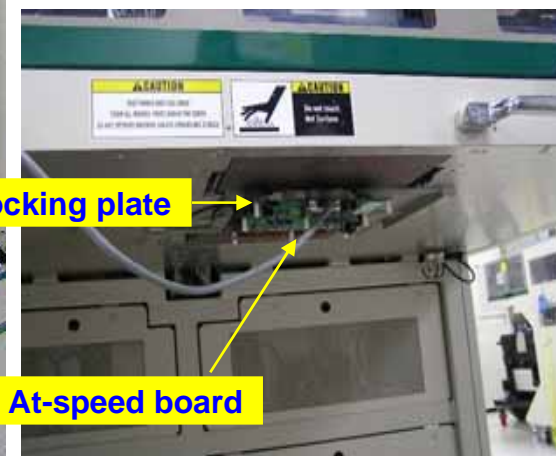
ASB (At Speed Board)

- Flowchart



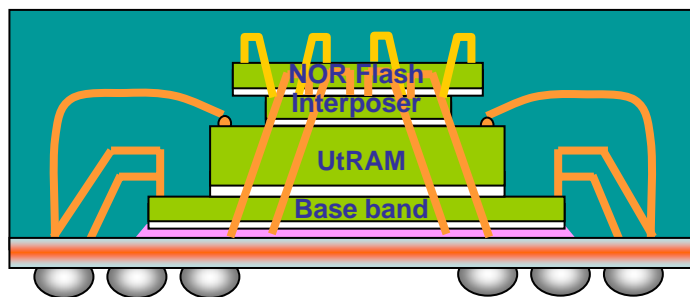
What is ASB?

- ASB (At Speed Board)
- Test machine introduction

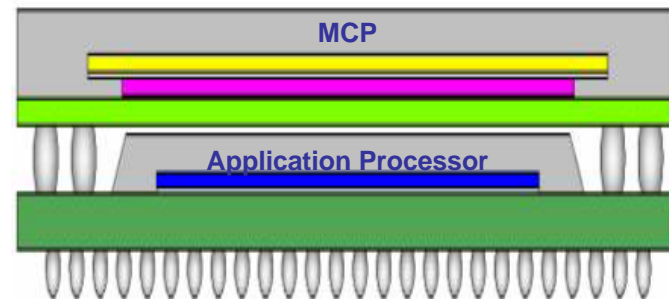


SiP type and needs

- SiP type and needs



Stack



POP

- Must guarantee W3 for memory/flash
Burn-in → High risk investment, capacity etc.
Temperature test → Low throughput etc.
Many test items → Capacity and investment

We need more powerful test methodology

Application of ASB in Memory test

❏ POP type package flow

- As of

Application processor Assembly

→ ATE Test

→ ASB Test

→ Stack (with MCP)

→ ATE Test (using memory tester)

→ ASB Test

→ Packing

- To be

Application processor Assembly

→ ATE Test

→ Skip

→ Stack (with MCP)

→ Skip (using memory tester)

→ ASB Test

→ Packing

Using ASB, we can guarantee POP's yield, speed, function etc and skip the memory test

Future plan

■ Stack type package flow

- As of

Base band & Memory Assembly

→ Memory Burn-In

→ Memory test (using memory tester)

→ Base band test (using Logic tester)

→ ASB Test

→ Packing

- To be

Base band & Memory Assembly

→ Skip

→ Skip

→ Base band test (Partial Skip)

→ ASB Test

→ Packing

ASB test is being tried instead of the memory burn-in, test and large size logic vectors etc.

Methodology to Skip the Memory Test Using ASB (At Speed Board)

Thanks !