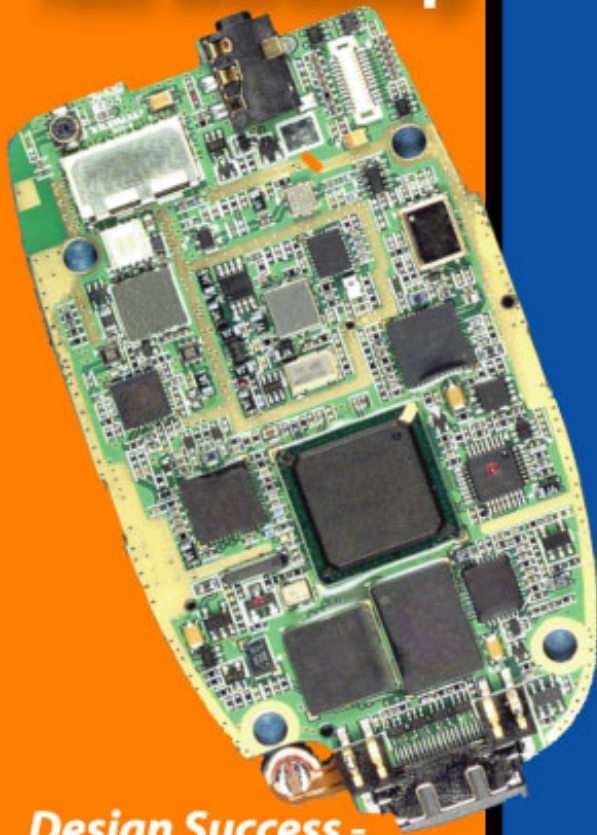


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Sept. 11-14, 2005 , Napa, CA

RF BIST Scheme for LNA in RF Systems

Bruce C. Kim

Associate Professor

The University of Alabama

12th Annual

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Outline

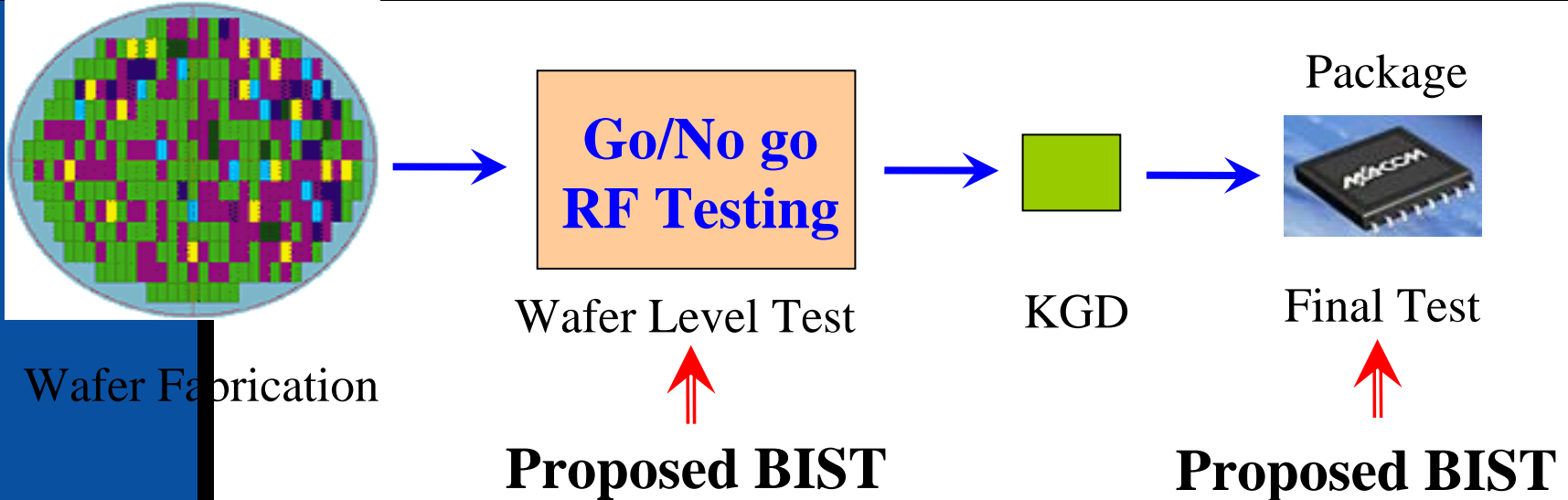
- **Objectives**
- **Proposed RF BIST**
- **Results**
- **Conclusions**

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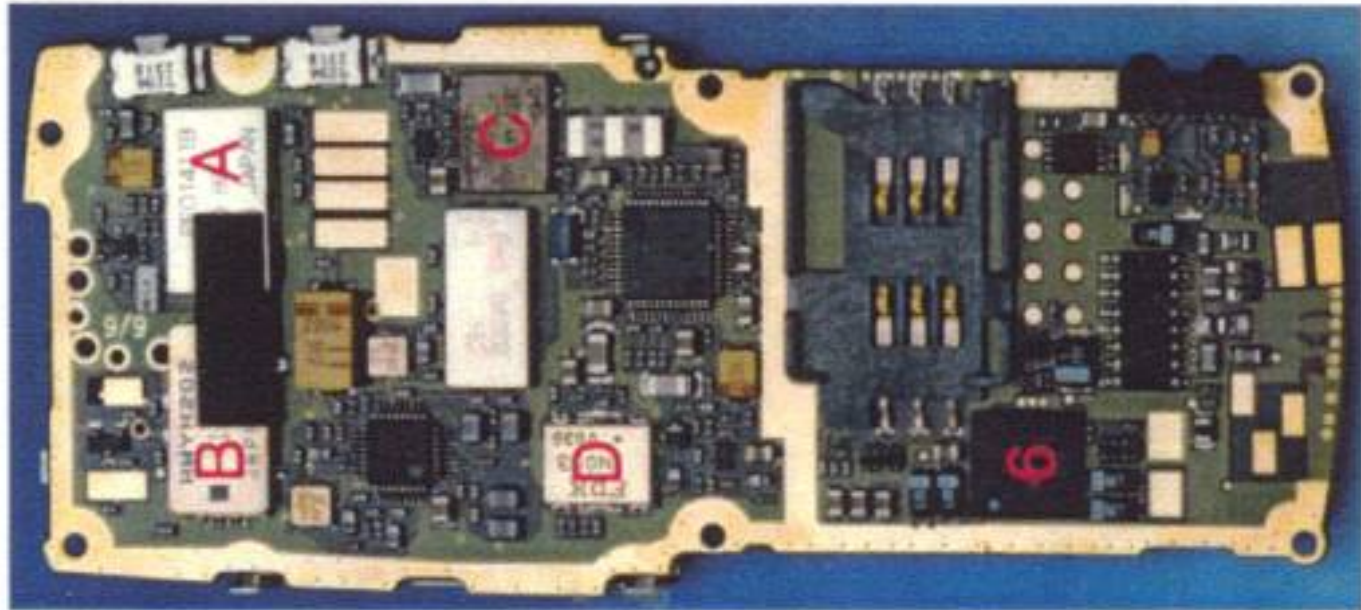
Objectives



- Propose a go-no go testing in the wafer level
- Propose to test at the packaged level for LNA specifications

Physical Parts of Cell Phone

Main Board (Bottom View)

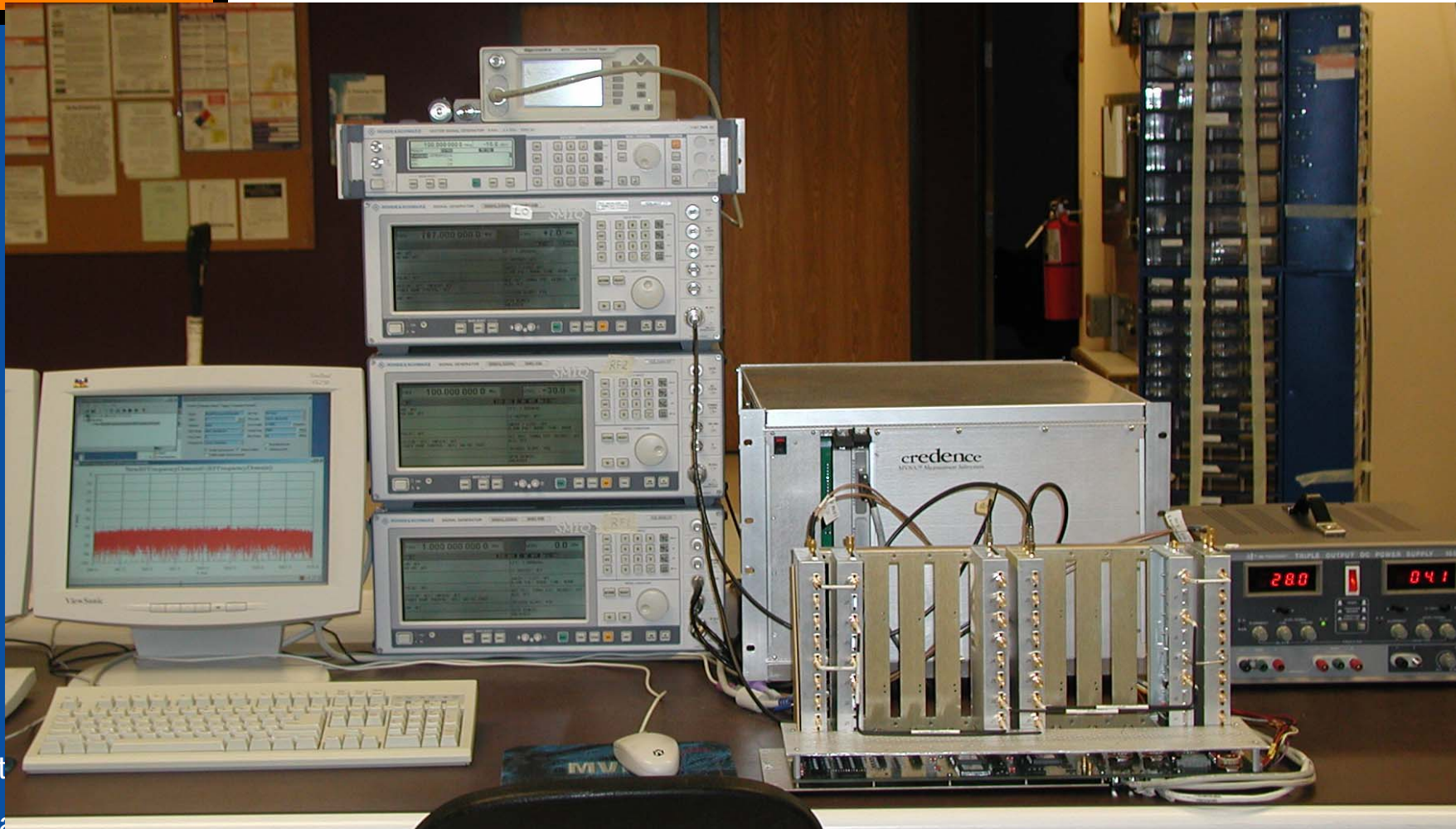


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RF Testing



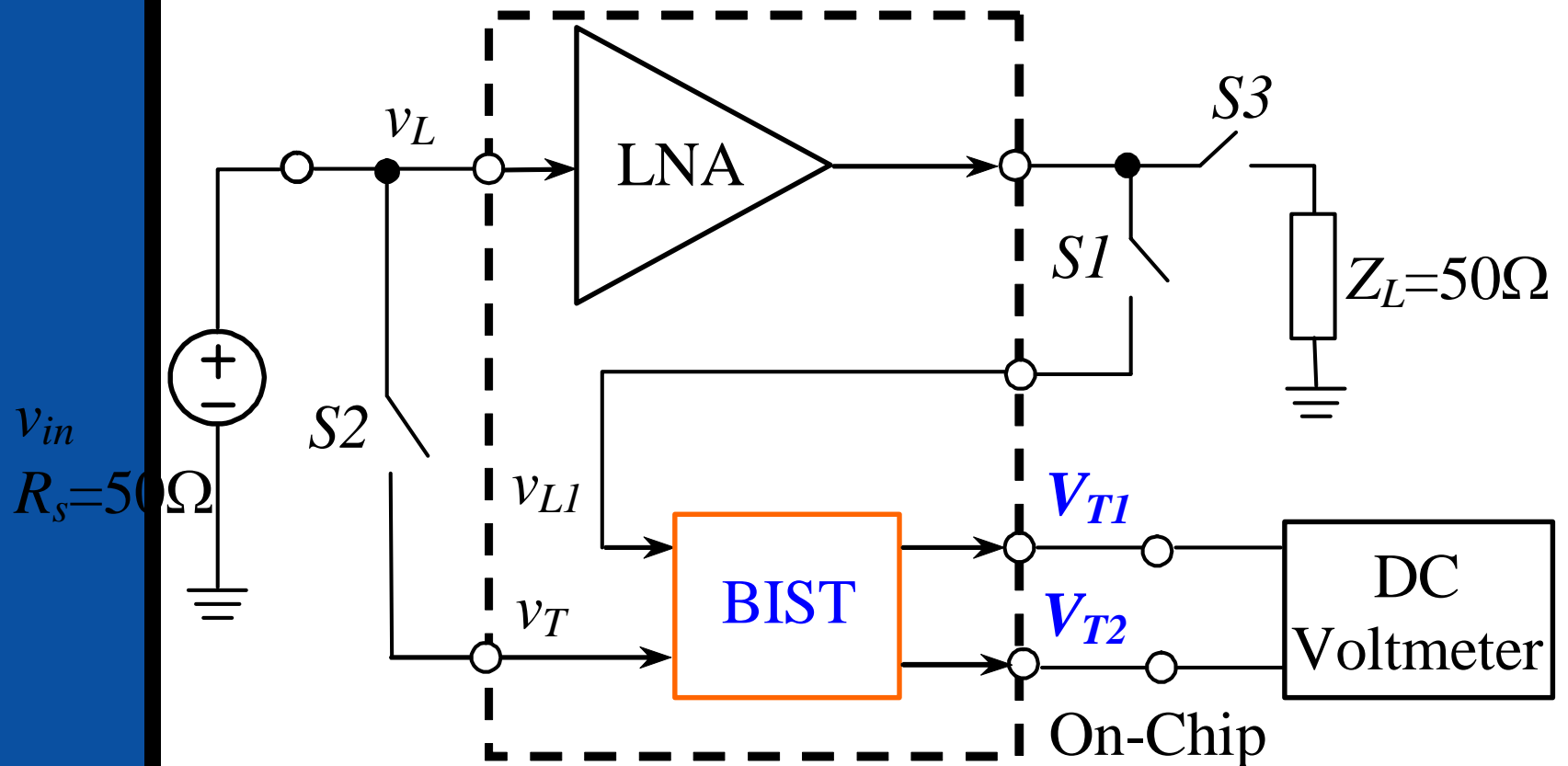
Test Technique Comparison

	Input Impedance/Gain/ Input Return Loss		Noise Figure	
	(1)	(2)	(1)	(2)
External Equipment	VNA Power Supply	DC Meter RF Source Power Supply	Noise Figure Analyzer (RF Spectrum Analyzer) RF Signal Generators Power Supply	DC Meter RF Source Power Supply
Test Cost	High	Low	High	Low
Resolution	High	High	High	High

(1) Current test technique

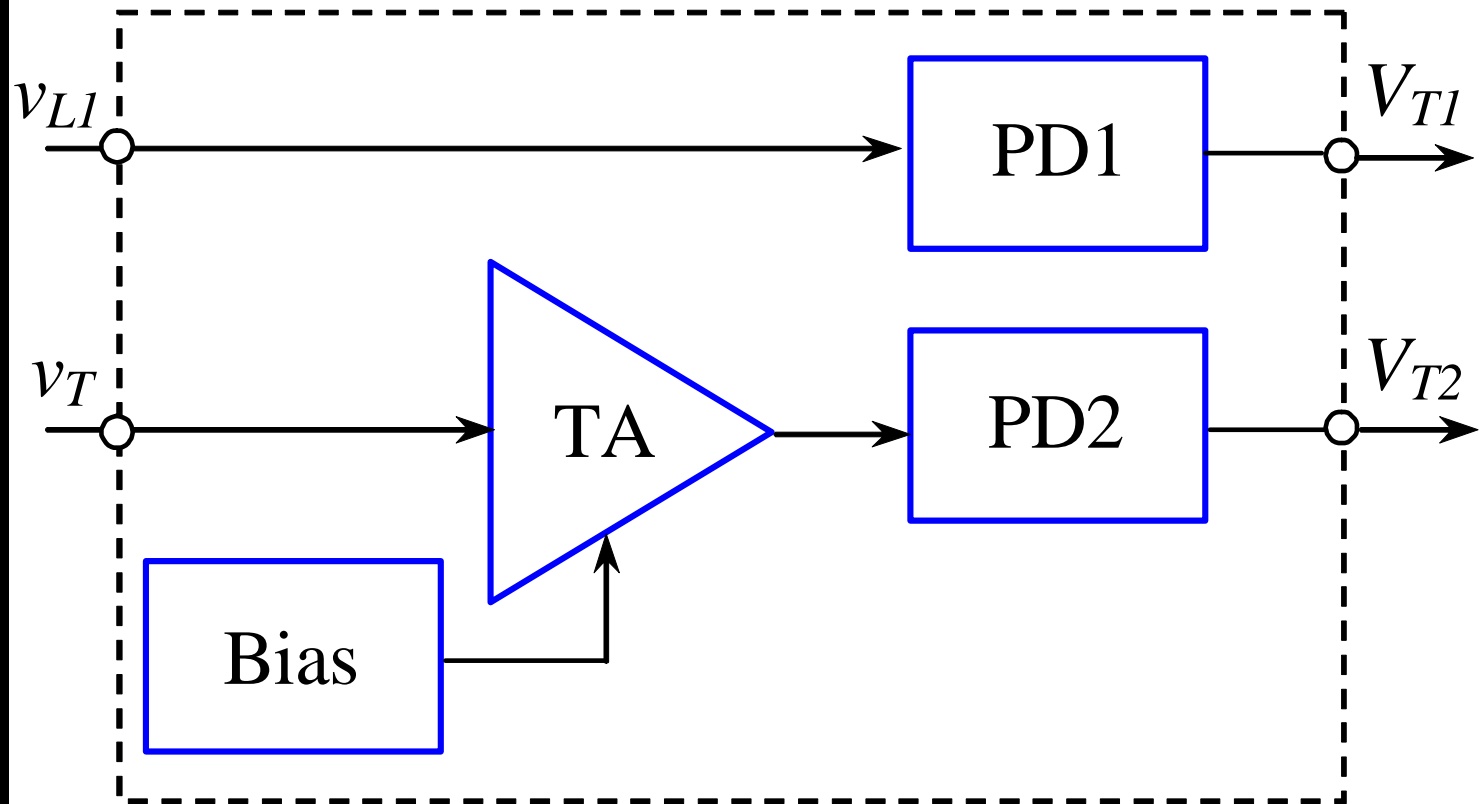
(2) Proposed BIST technique

Proposed RF BIST for LNA



- ✓ **S1 closed:** Measure V_{T1}
- ✓ **S2 & S3 closed:** Measure V_{T2}

Proposed RF BIST Hardware

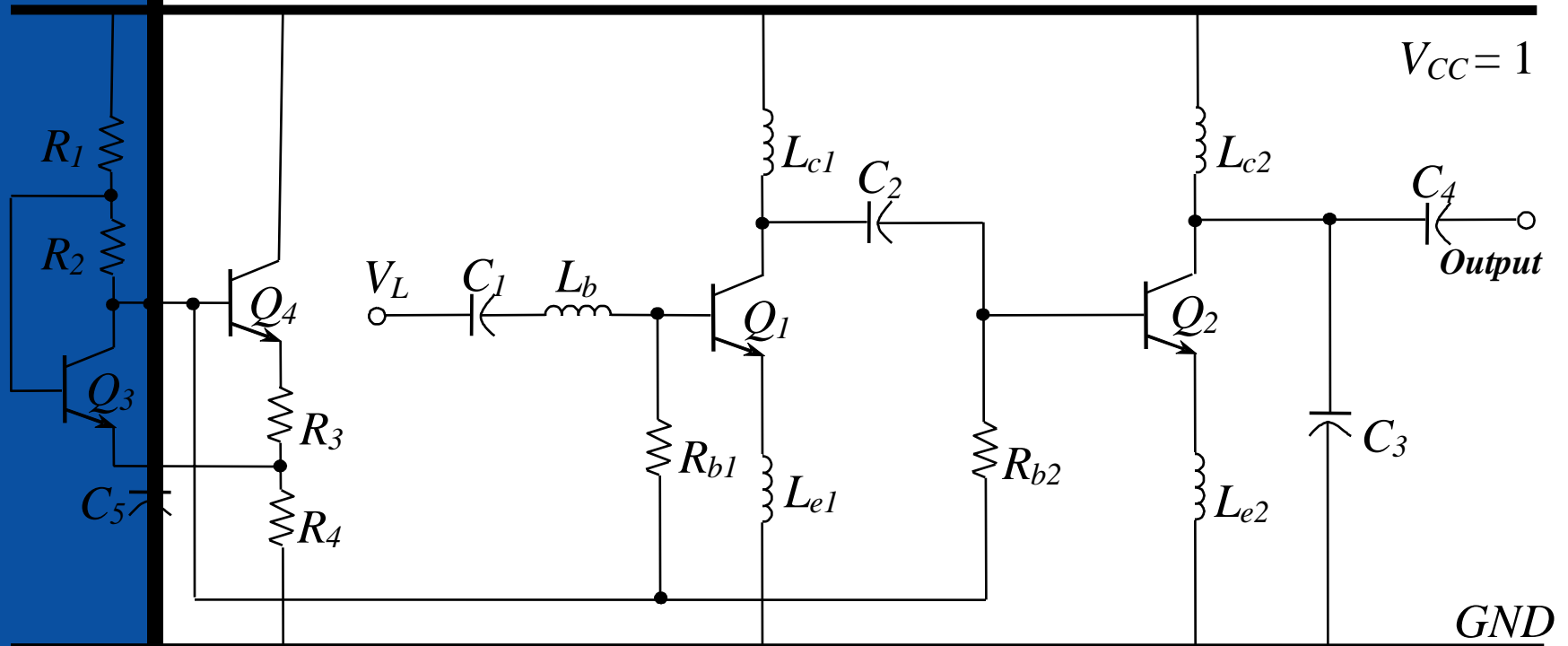


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5GHz Low Noise Amplifier



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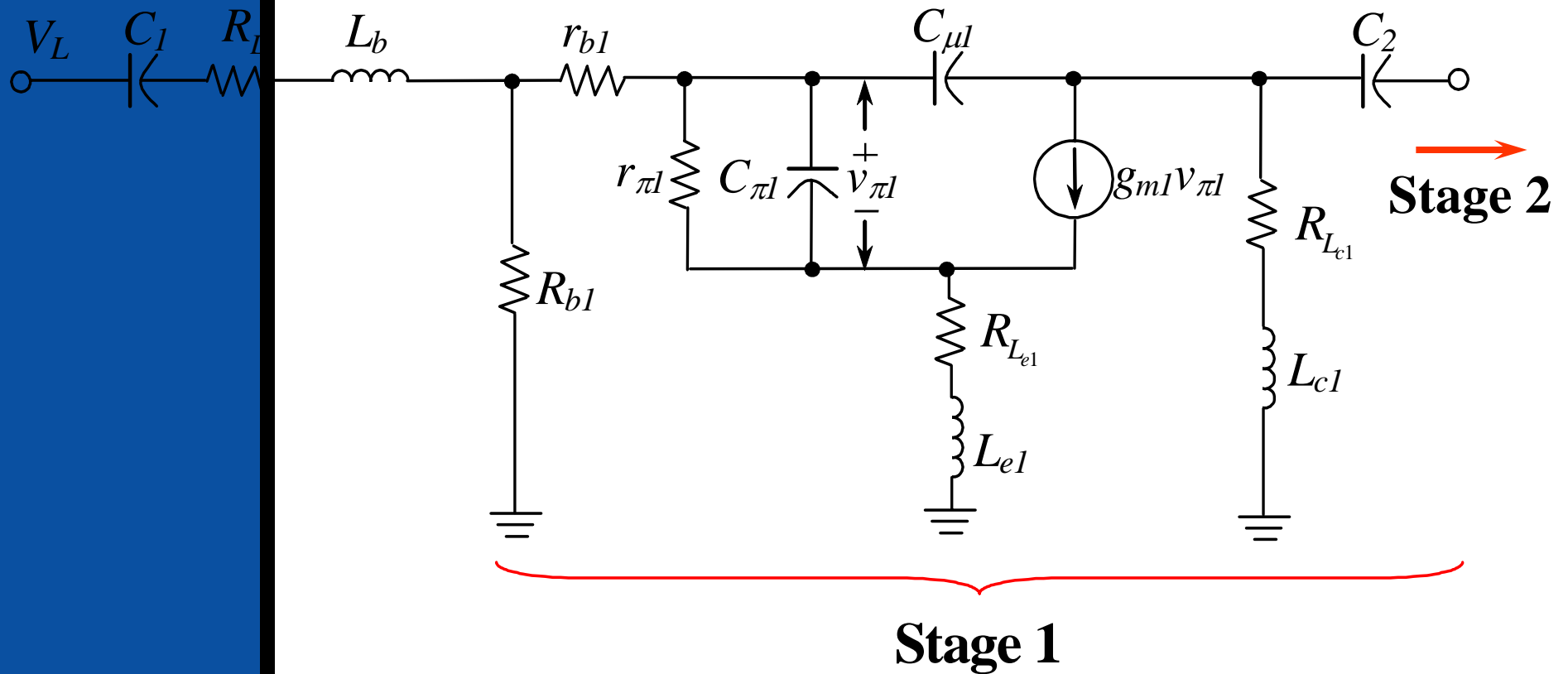
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0.18 μ m SiGe HBT Technology

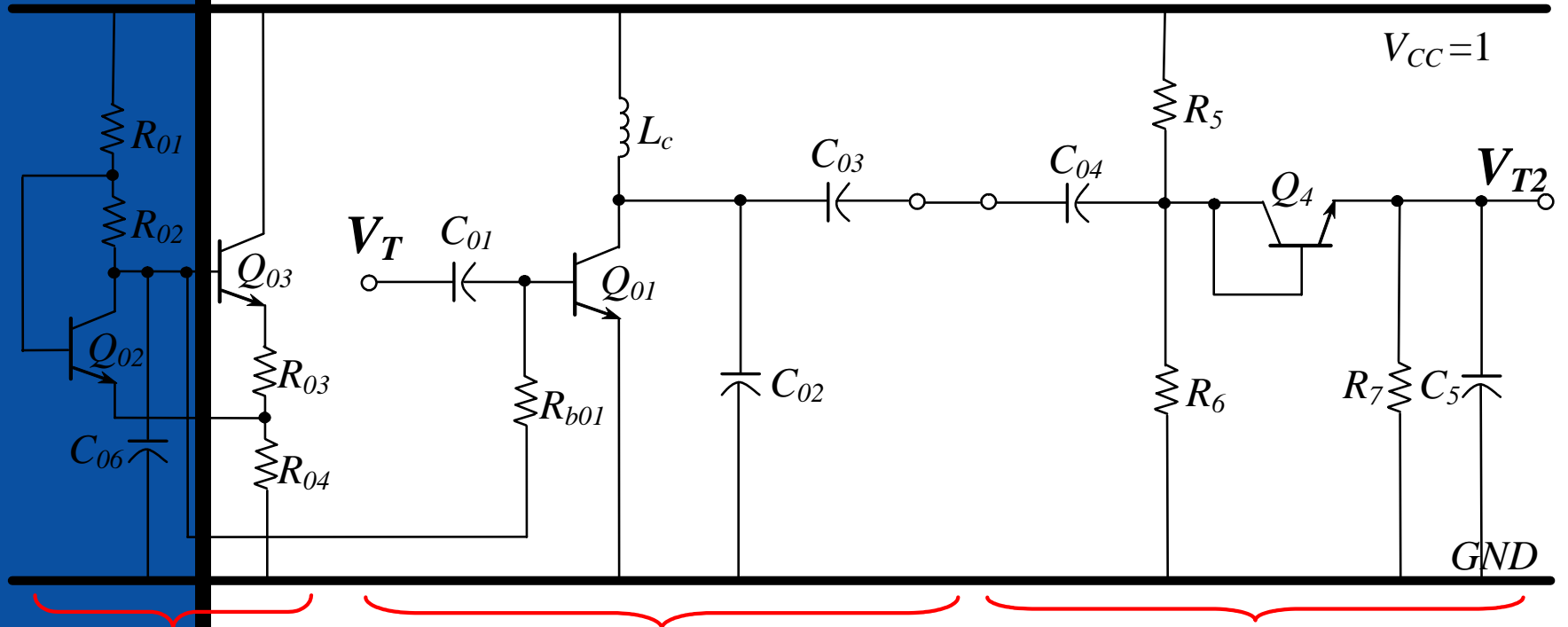
Band gap reference

Amplifier

Small-Signal Model for LNA



RF BIST Circuit



Band-gap reference

Test Amplifier

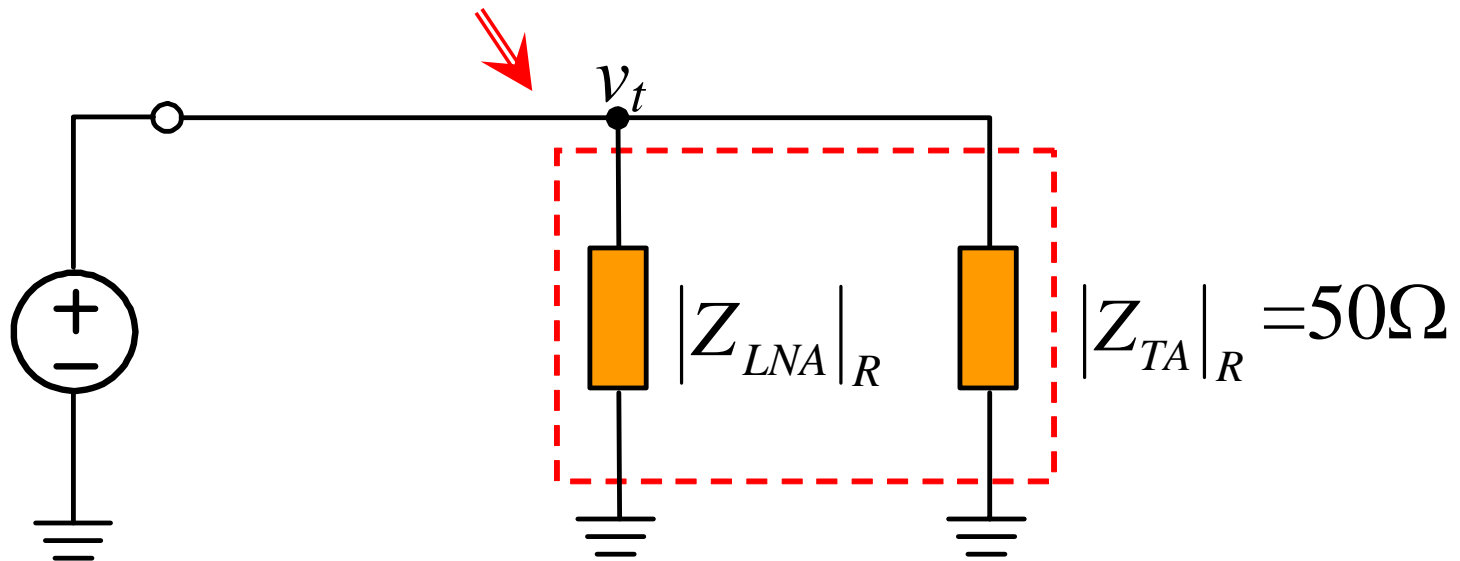
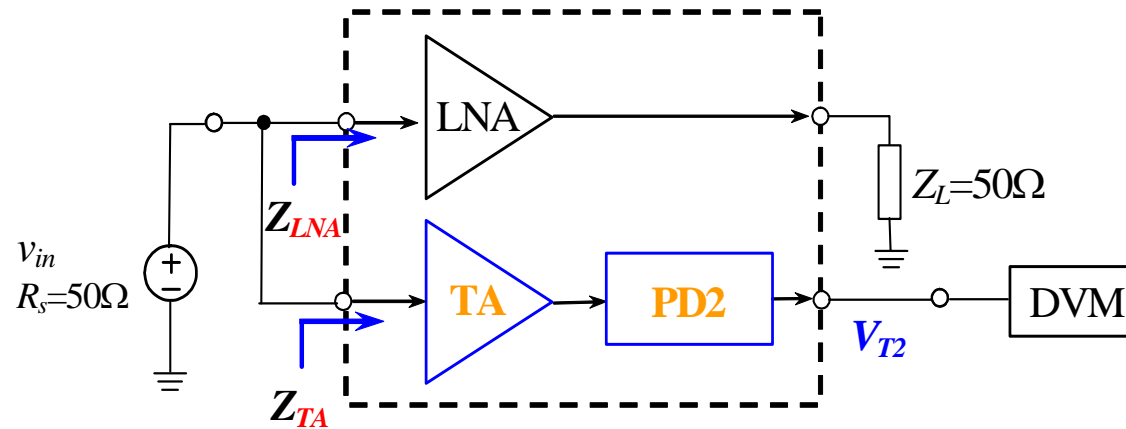
Peak Detector2

□ Validation Procedure

✓ $Gain = V_{T2} / V_T = 3$

✓ Test V_{T2} for $Gain=3$

Equivalent Circuit Model



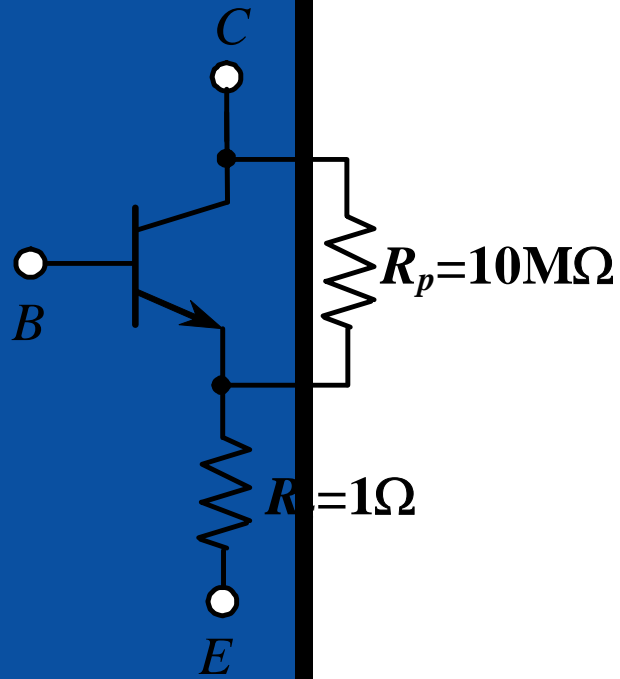
V_{in}
 $R_s=50\Omega$

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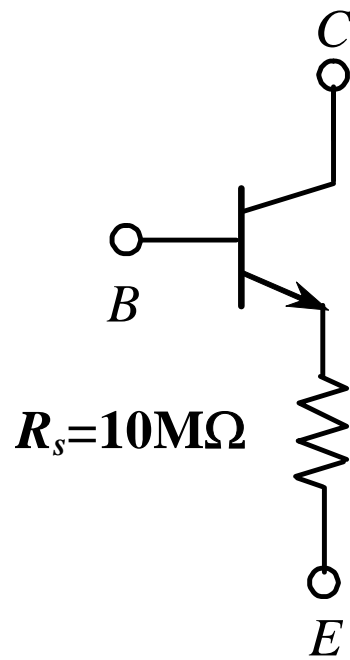
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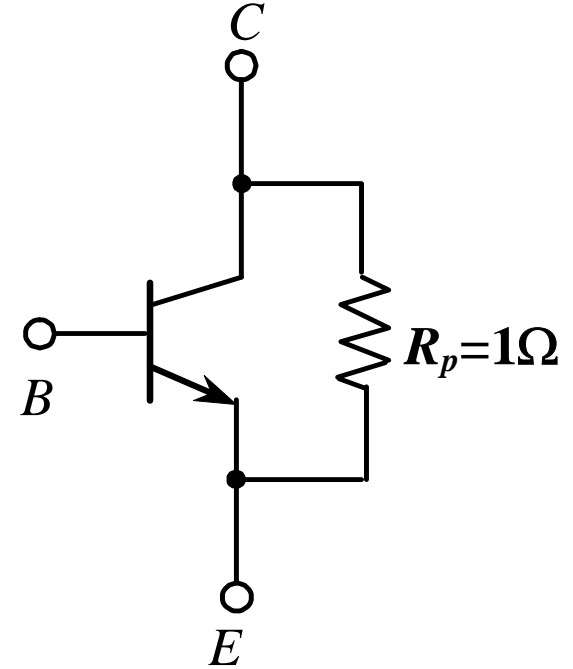
Defect Models



(a) Defect-free

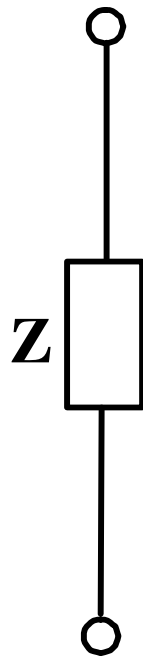


(b) Open Defect

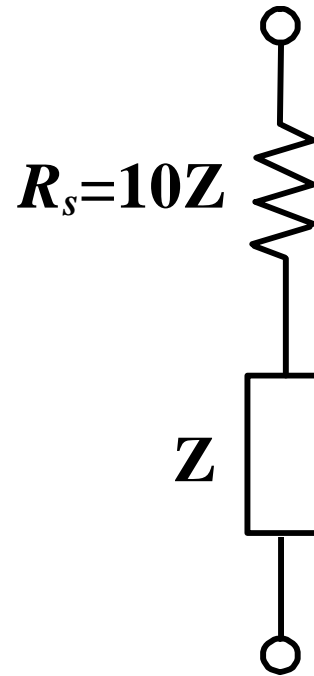


(c) C-E Short Defect

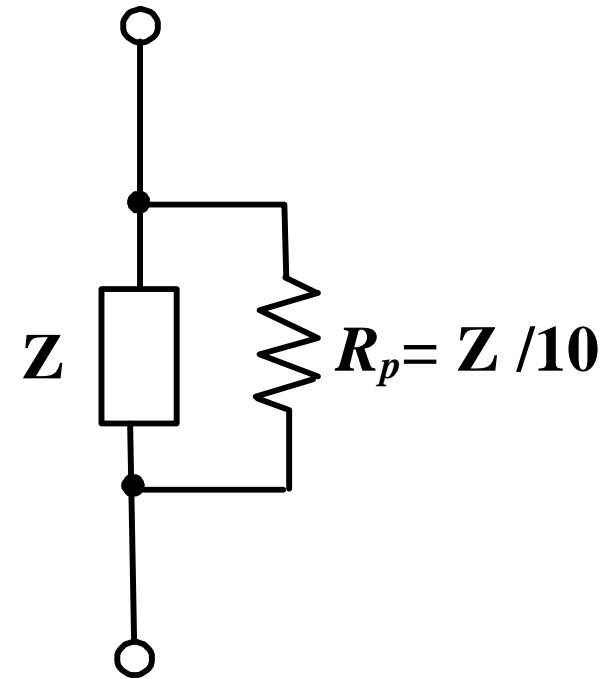
Defect Models for Passives



(a) Defect-free

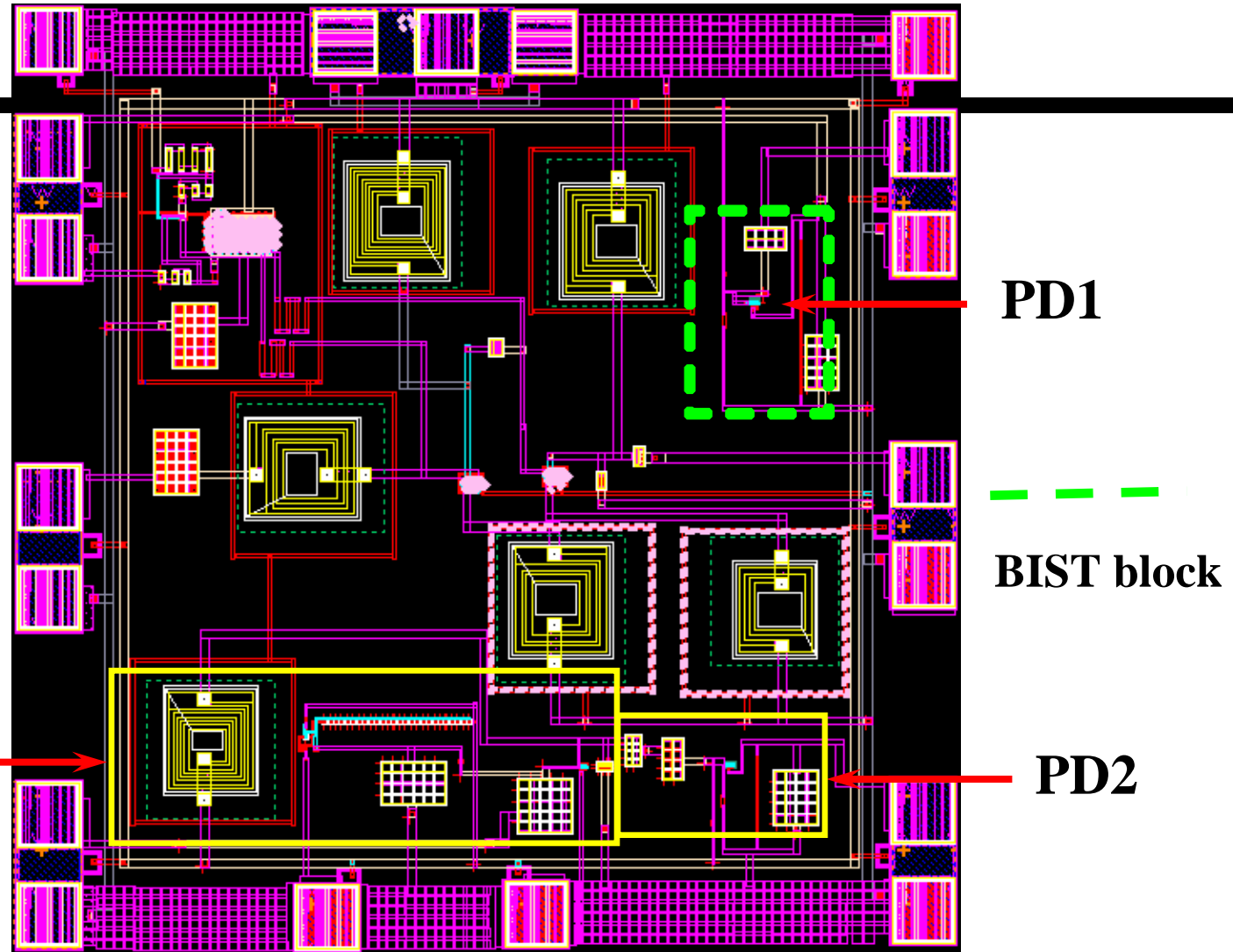


(b) Open Defect



(c) Short Defect

Chip Layout



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Mathematical Expressions

- Magnitude of Input Impedance
- Gain
- Noise Figure
- Input Return Loss

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Fault-Free Input Impedance

$$\left| Z_{LNA} \right|_R = R_s \frac{K_1}{1 - \left(1 + \frac{R_s}{Z_2} \right) K_1} [\Omega]$$

$$K_1 = G_1 / G_2$$

$G_1 = f(V_{T2}, v_{in})$: Voltage gain of BIST

G_2 : Voltage gain of Test Amplifier

Faulty-Case Input Impedance

Case
1:

$$V_{MT2} > V_{RT2},$$

$$\left| Z_{LNA} \right|_M \leq R_s \frac{K_1}{1 - \left(1 + \frac{R_s}{Z_2} \right) K_1} [\Omega]$$

Case
2:

$$V_{MT2} \leq V_{RT2},$$

$$\left| Z_{LNA} \right|_M \leq K_1 \left(2 \left| Z_{LNA} \right|_R + R_s \right) [\Omega]$$

V_{MT2} , $\left| Z_{LNA} \right|_M$ replace V_{T2} , $\left| Z_{LNA} \right|$ under a faulty case, respectively.

Fault-Free Voltage Gain

$$G_{LNAR} = \left(1 + \frac{R_s}{|Z_{LNA}|_R} \right) G_3$$

$G_3 = f(V_{T1}, v_{in})$: Voltage gain of BIST

Faulty-Case Voltage Gain

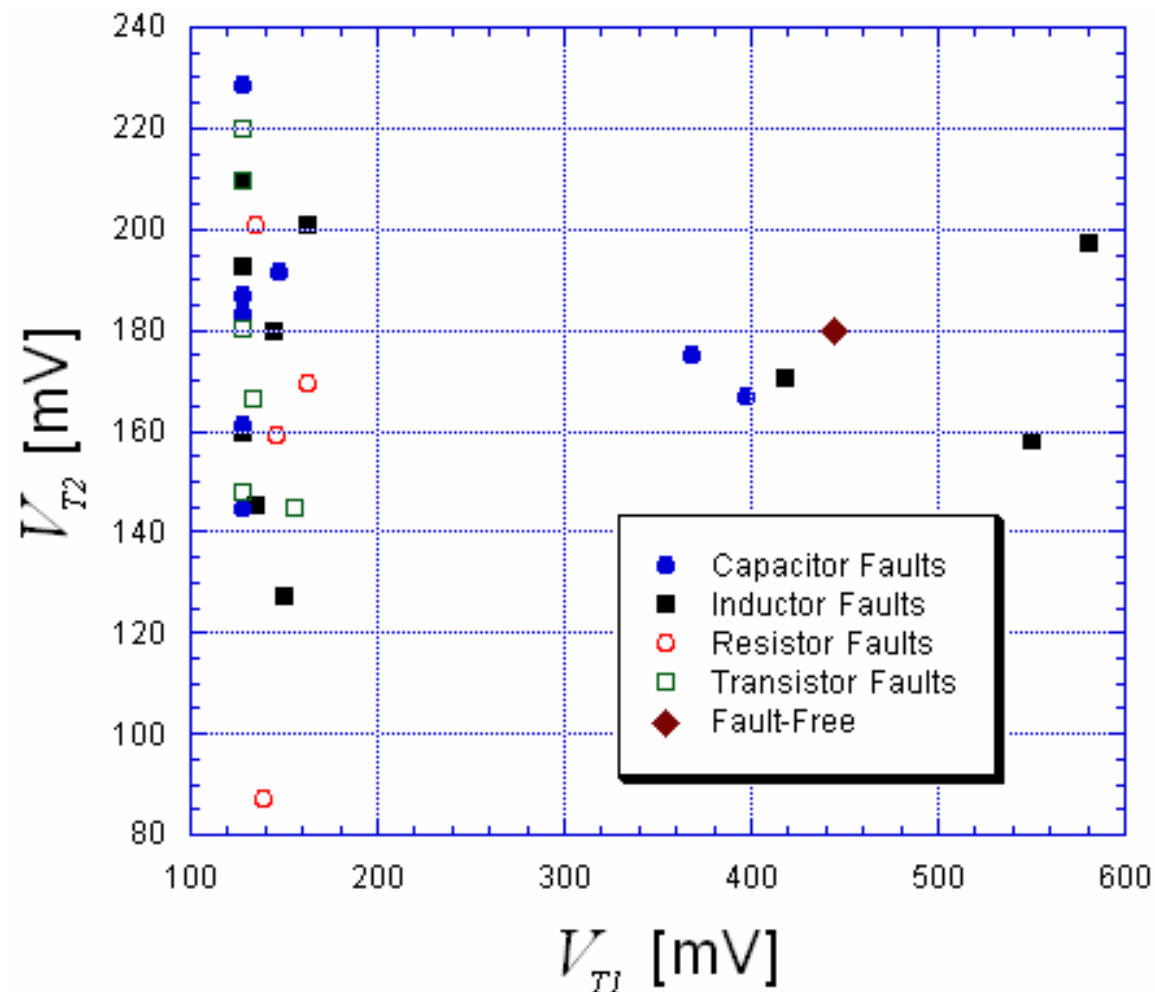
Case 1: $V_{MT2} > V_{RT2}$,

$$G_{LNA M} \leq \left(1 + \frac{R_s}{|Z_{LNA}|_{\min M}} \right) G_3$$

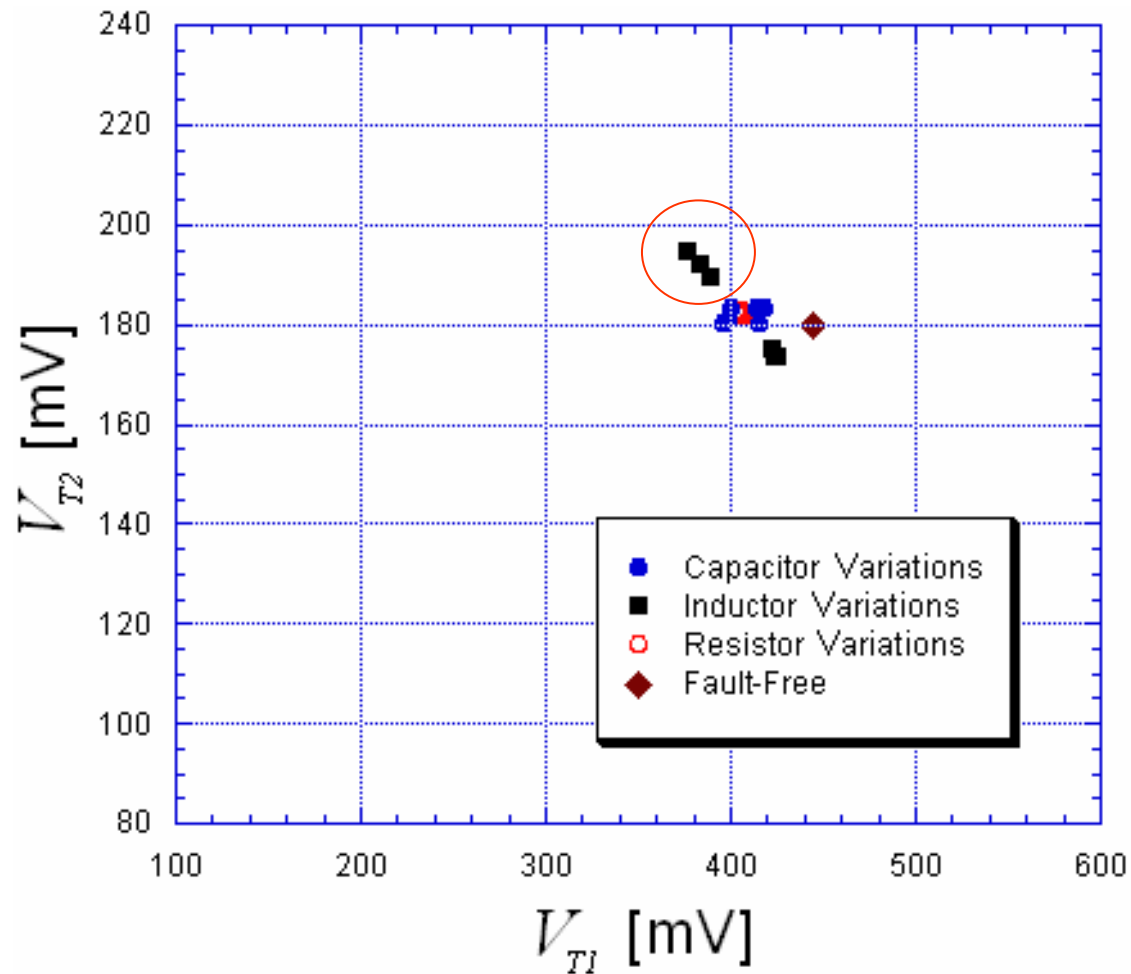
Case 2: $V_{MT2} \leq V_{RT2}$,

$$G_{LNA M} \leq \frac{|Z_{LNA}|_R + R_s}{|Z_{LNA}|_{\max M}} G_3$$

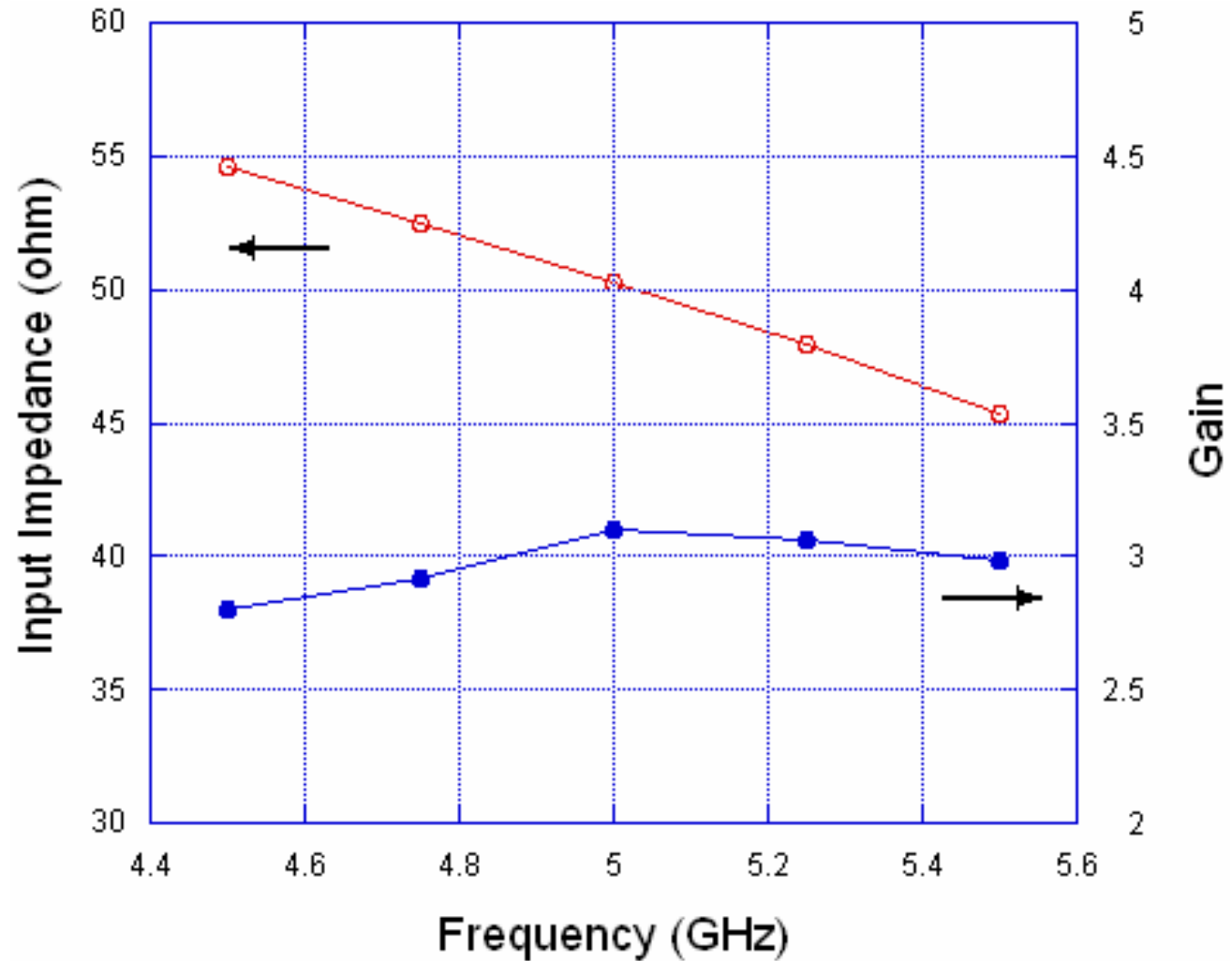
DC Outputs for Catastrophic Faults



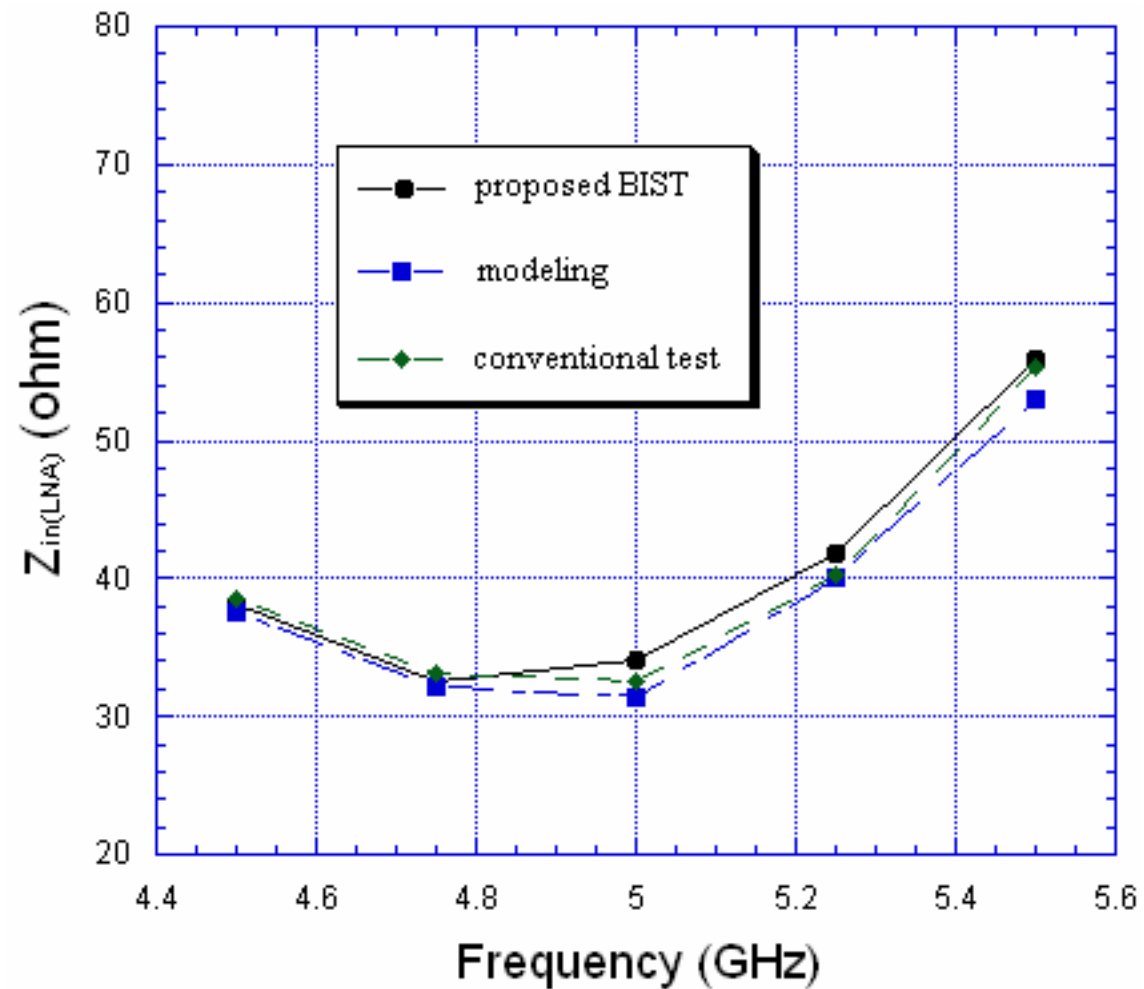
Parametric Variations



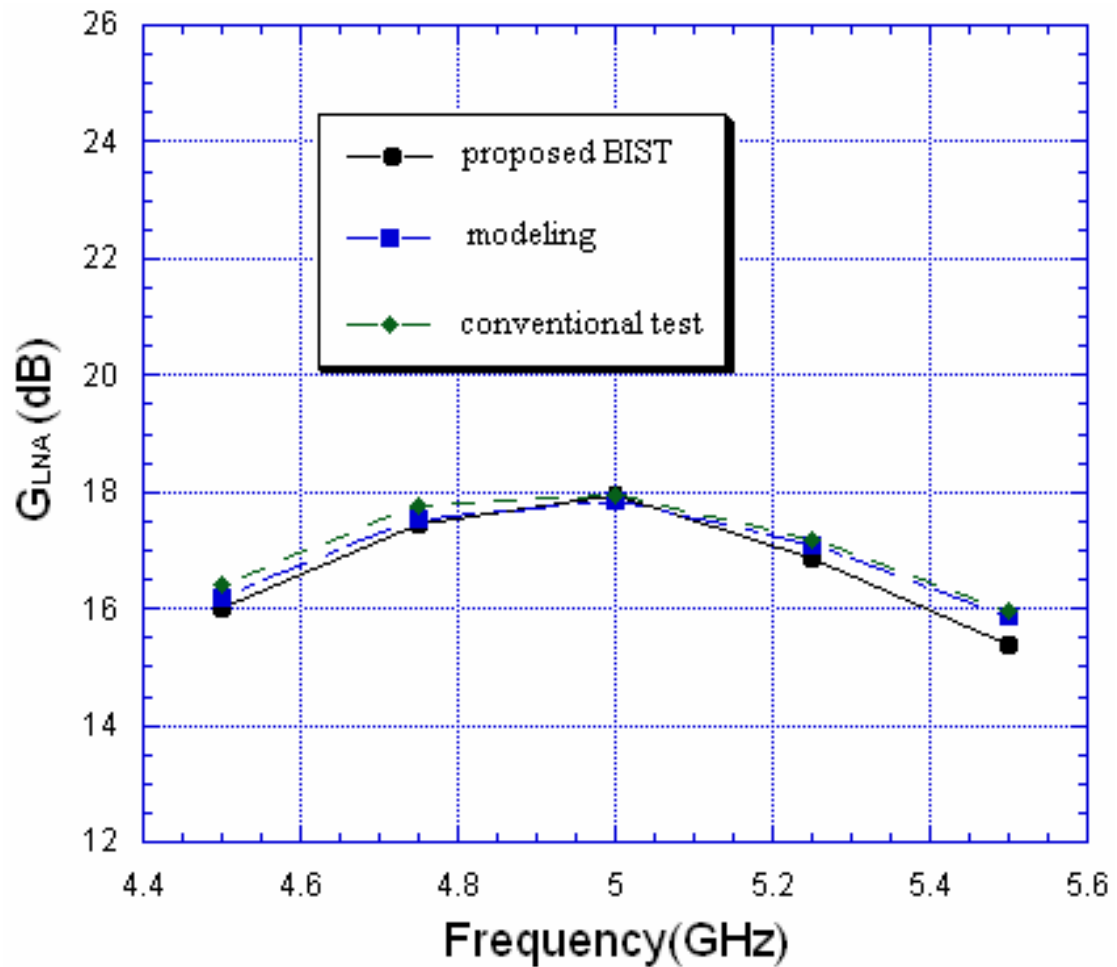
Test Results for GAIN and Impedance



Input Impedance Results



Gain Results



Fault-Free Noise Figure

$$NF_R = 1 + \left\{ \frac{|Z_{LNA}|_R}{R_s + |Z_{LNA}|_R} \right\}^2 \cdot \frac{G_0}{G_3^2} (NF_0 - 1)$$

G_0 : power gain required by specification

NF_0 : noise figure required by specification

Faulty-Case Noise Figure

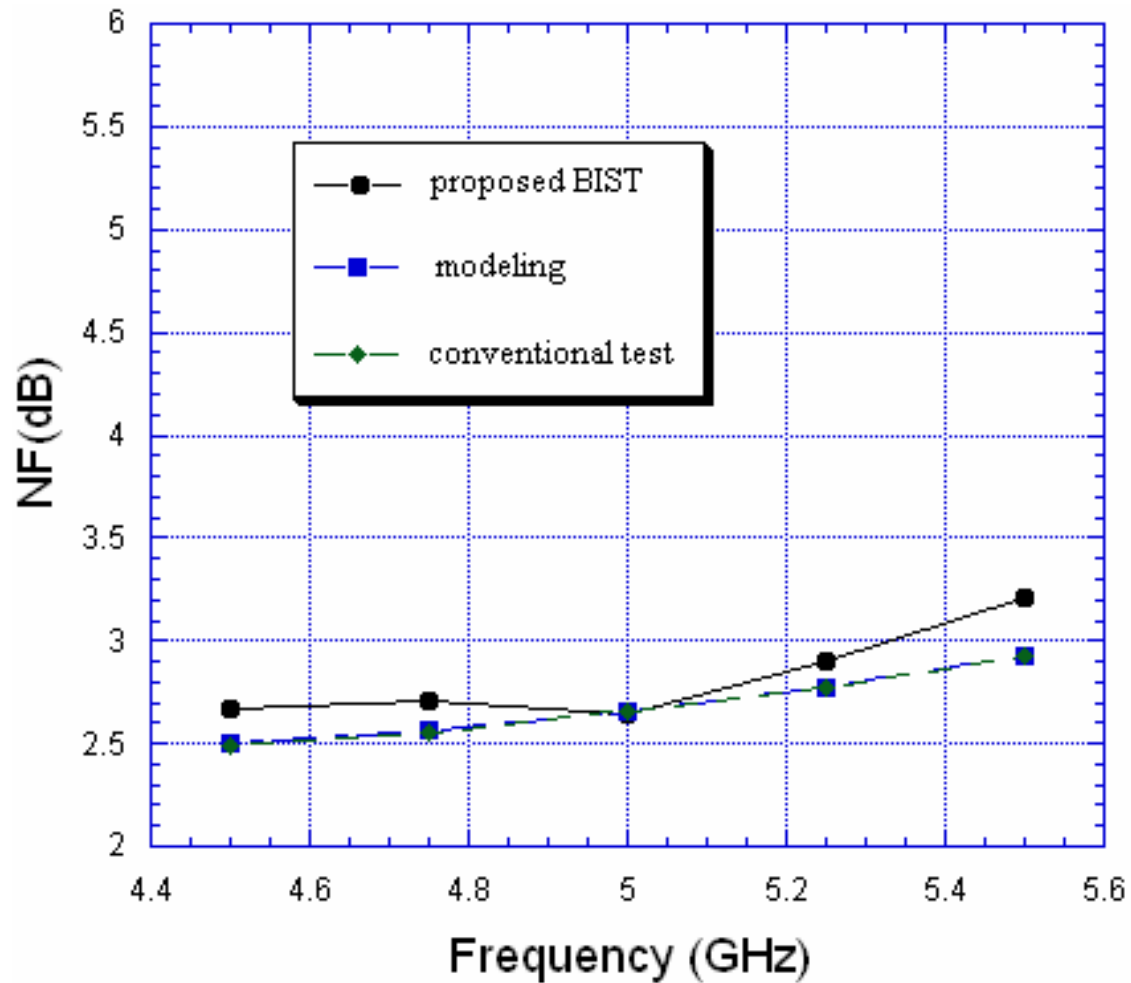
Case 1: $V_{MT2} > V_{RT2}$,

$$NF_M \geq 1 + \frac{|Z_{LNA}|_{\min M}^2 G_0}{\left(|Z_{LNA}|_{\min M} + R_s\right)^2 G_3^2} (NF_0 - 1)$$

Case 2: $V_{MT2} \leq V_{RT2}$,

$$NF_M < 1 + \frac{|Z_{LNA}|_{\min M}^2 G_0}{\left(|Z_{LNA}|_{\min M} + R_s\right)^2 G_3^2} (NF_0 - 1)$$

Noise Figure Results



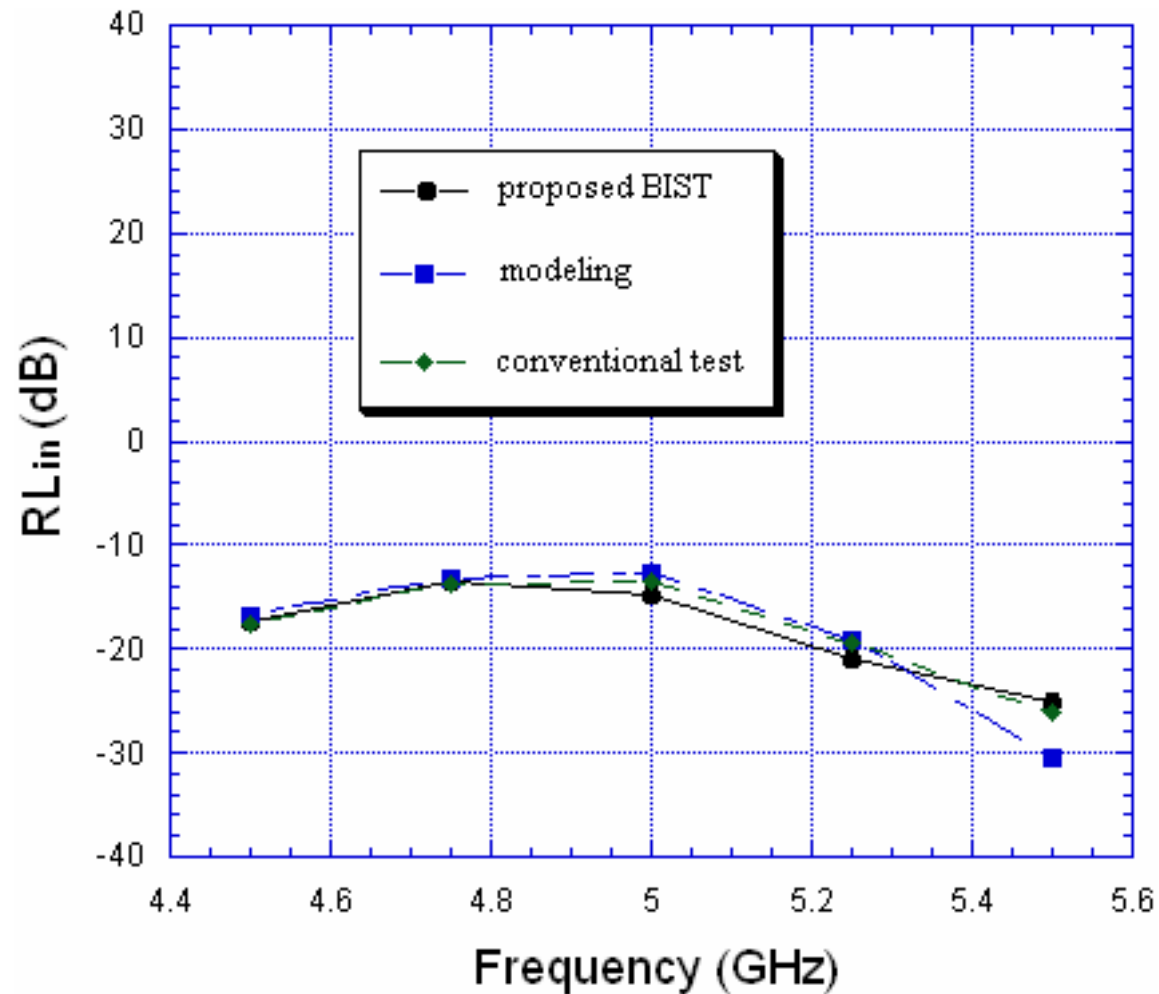
Fault-Free Input Return Loss

$$RL_{inR} = 20 \log \left| \frac{|Z_{LNA}|_R - Z_0}{|Z_{LNA}|_R + Z_0} \right|$$

RL_{inR} : Input Return Loss of BIST

$$Z_0 = 50\Omega$$

Input Return Loss Results



Data Summary

Test Faults	External Equipment Test				Proposed On-Chip BIST			
	(1)	(2)	(3)	(4)	(1)	(2)	(3)	(4)
Fault-free	40.26	17.15	2.773	-19.4	41.76	16.89	2.904	-20.9
<i>Q_I</i> Base Open	92.87	-75.84	88.06	-10.5	70.88	-44.44	61.11	-12.9
<i>L_b</i> + 30%	53.38	16.18	2.956	-29.7	49.01	14.95	3.960	-26.7

- (1) Input Impedance [Ω]
- (2) Gain [dB]
- (3) Noise Figure [dB]
- (4) Input Return Loss [dB]

Limitations

Parameters	LNA specifications	Using proposed BIST
Input Impedance [Ω]	50	✓
Voltage Gain [dB]	> 10	✓
Noise Figure [dB]	< 3	✓
Return Loss [dB]	< -10	✓
IIP3 [dBm]	> 0	×

Conclusions

- ❖ Designed new RF BIST hardware for 5.25GHz LNA
- ❖ Utilized input impedance and DC voltage measurements
- ❖ Simple and inexpensive