

# RF BIST Scheme for Low Noise Amplifier in RF Systems

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**ABSTRACT:** This paper presents a new low-cost RF Built-In Self-Test (BIST) circuit for measuring RF parameters for 5.25GHz low noise amplifier (LNA). The BIST circuit is designed using 0.18 $\mu\text{m}$  SiGe technology. The test technique using BIST circuit utilizes input impedance matching and output transient voltage measurements. A set of derived mathematical equations are used to calculate RF parameters from low-cost DC measurements. The entire concept is low-cost due to using DC measurements rather than using traditional RF measurements for RF parameters.

## I. INTRODUCTION

Recent proliferations of RFIC chips have been overwhelming with rapid growth in RF system integration of wireless communications. The integration density and complexity of these devices increase with consumer demands in functionality. With test cost of 40% of the total product cost, there should be a low cost way to test RFIC chips. In spite of the considerable research underway to reduce the test overhead in RFIC chips, the difficulties in testing still remain to be the major bottleneck of the product manufacturing. The problems come from the limited access to major components of the internal RF structures and the non-linear effects in RF faults may cause on a circuit under test. To solve these problems, the Built-In Self-Test (BIST) technique in the RF domain is applied as a suitable test structure on the chip [1-5].

## II. APPROACH

Traditional method to test LNA involves measurements of S-parameters, noise figure, SNR and IIP3 using variety of expensive RF test equipment. Our approach utilizes on-chip BIST circuit to measure important LNA specifications without major external test equipment.

The proposed BIST circuit is shown in Figure 1. It consists of test amplifier (TA) and peak detector (PD2) circuit stages. The other peak detector circuit (PD1) is also a part of the BIST circuit and it has the same topology as the PD2 circuit shown in Figure 1. The RF peak detectors are used to convert RF signal to DC voltage [6]. To reduce the output ripple voltage,  $R_{07}$  and  $C_{05}$  are chosen with large values.

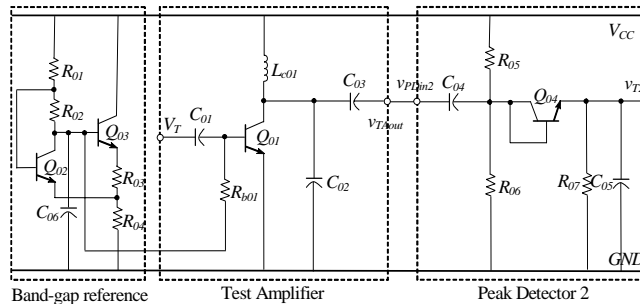


Figure 1. Circuit Schematic of RF BIST.

Figure 2 shows the test structure which measures gain, noise figure, input impedance, and input return loss. It consists of the RF voltage source generator ( $v_{in}$ ), LNA chip with RF BIST, DC meter, 50 ohm load impedance ( $Z_L$ ), and mechanical switches ( $S1$ ,  $S2$  and  $S3$ ). The RF BIST consists of test amplifier (TA) and two RF peak detectors (PD1 and PD2).

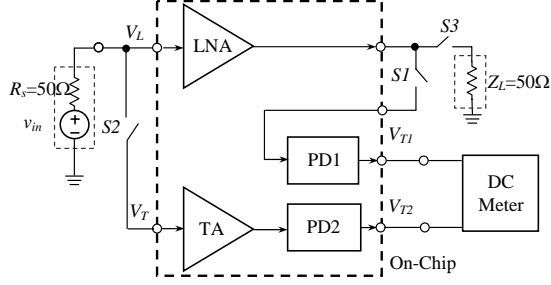


Figure 2. Test Set-up of Prototype LNA.

### A. Input Impedance

Figure 4 shows the equivalent circuit for the inputs of the LNA and test amplifier.  $Z_1$  and  $Z_2$  represent the input impedance of the LNA and test amplifier, respectively. These impedances have real and imaginary parts.

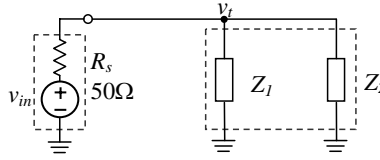


Figure 3. Equivalent Circuit of LNA Input.

First, we consider fault-free LNA with good input matching condition. The Equation (1.1) represents the theoretical values for the voltage across the input impedances of the LNA and TA. The TA is designed at 5GHz with the input and output matching impedances of  $50\Omega$ , and a flat gain of  $G_2 \approx 3$  to increase test output voltage to the original input voltage level  $|v_{in}|$  as indicated in Equation (1.2). The BIST circuit monitors the transient dc voltage  $V_{T2}$  as shown in Figure 3. Equations (1.1) and (1.2) represent important expressions that are developed to derive input impedance of the LNA.

$$|v_i| = \left| \frac{Z_1 // Z_2}{[R_s + (Z_1 // Z_2)]} \right| |v_{in}| = \left| \frac{Z_1}{2Z_1 + R_s} \right| |v_{in}| \quad (1.1)$$

$$\begin{aligned} V_{T2} &= |v_{TAout}| + V_{02} = |v_i| \times (G_2 \approx 3) + V_{02} \\ &= \left| \frac{Z_1}{2Z_1 + R_s} \right| |v_{in}| \times (G_2 \approx 3) + V_{02} \end{aligned} \quad (1.2)$$

where  $|Z_1|$  and  $|Z_2|$  are magnitudes of input impedances of LNA and TA, respectively,  $G_2$  is voltage gain of TA and  $V_{02}$  is dc output voltage of the peak detector, PD2.

The LNA and test amplifier are designed at 5GHz, so they have good matching condition at this frequency. However, at *TFR*, there are certain variations in magnitudes of input impedance of both LNA and test amplifier because of changes in their input matching condition. The test amplifier was designed by less than  $\pm 10\%$  magnitude variation of input impedance at *TFR* as compared to magnitude of input impedance at 5GHz. When this approximation is applied,  $|Z_2| \approx \text{Re}(Z_2)$  for  $\text{Re}(Z_2) \gg \text{Im}(Z_2)$ . From Equations (1.1) to (1.2) and this approximation, we can express the new magnitude of input impedance of LNA as

$$|Z_{1B}| = R_s \frac{K_1}{1 - \left(1 + \frac{R_s}{K_2}\right) K_1} [\Omega] \quad (2.1)$$

where  $K_1 = G_{02} / (G_2 \pm \Delta G_2)$  and  $G_{02}$  is the voltage gain obtained by the input matching test.  $K_2 = |Z_2| \pm \Delta |Z_2|$ ,  $\Delta G_2$  and  $\Delta |Z_2|$  are gain and magnitude variations of input impedance of test amplifier, respectively.

$$G_{o2} = \frac{V_{T2} - V_{o2}}{|V_{in}|} \quad (2.2)$$

Now let's consider faulty case. The LNA can have catastrophic faults such as resistive short and open faults due to the spot defects, and parametric faults such as unusual parameter variations and unusual process variations [1, 3]. In this case, there is also a certain variation in magnitude of input impedance of LNA because of change in its input matching condition. If the transient output voltage has  $\overline{V_{T2}} > V_{T2}$ , Equation (2.1) can be expressed as Equation (3).  $\overline{V_{T2}}$  replaces  $V_{T2}$  under a faulty case.

$$|\overline{Z_{1B}}| \leq |Z_{1B}| [\Omega] \quad (3)$$

where  $|\overline{Z_{1B}}|$  represents  $|Z_{1B}|$  under a faulty case.

If  $\overline{V_{T2}} \leq V_{T2}$ , Equation (2.1) can be expressed as Equation (4).

$$|\overline{Z_{1B}}| \leq K_1 (2|Z_{1B}| + R_s) [\Omega] \quad (4)$$

### III. RESULTS

Table 1 lists gain and input impedance of test amplifier. These results are used to obtain magnitudes of input impedances of the LNA at *TFR* as shown in Equation (2.1). Because the test amplifier is designed with  $\text{Re}(Z_2) \gg \text{Im}(Z_2)$  at *TFR*, phase shift for input impedance of test amplifier at this frequency range can be neglected.

Table 1. Gains and input impedances of test amplifier.

Frequency [GHz]	S-Parameter Results	
	$G_2 \pm \Delta G_2$	$ Z_2  \pm \Delta  Z_2 $ [ $\Omega$ ]
4.50	2.80	54.57
4.75	2.92	52.45
5.00	3.10	50.28
5.25	3.06	47.95
5.50	2.98	45.31

The transient voltages ( $V_{T1}$  and  $V_{T2}$ ) are measured after 40 nanoseconds settling time of the peak detectors, PD1 and PD2 to ensure steady-state DC value. The output RC time constant of the peak detector contributed to the settling time constant. We used RF input source of 100mV to 180mV at 4.5-5.5GHz. The DC voltages  $V_{T1}$  and  $V_{T2}$  are measured using a conventional DC meter.

From these DC voltage measurements, we calculated real RF parameters. Table 2 compares results of external equipment test and proposed on-chip BIST for fault-free LNA as a function of frequency. Our proposed BIST results showed very close results compared to external equipment test.

Table 2. Comparison between two techniques.

Freq. [GHz]	External Equipment Test				Proposed On-Chip BIST			
	$ Z_i $ [ $\Omega$ ]	$G_I$ [dB]	$NF$ [dB]	$RL_{in}$ [dB]	$ Z_{1B} $ [ $\Omega$ ]	$G_{1B}$ [dB]	$NF_B$ [dB]	$RL_{inB}$ [dB]
4.50	38.45	16.40	2.493	-17.68	38.16	16.00	2.674	-17.44
4.75	33.08	17.76	2.559	-13.82	32.64	17.44	2.707	-13.56
5.00	32.57	17.95	2.652	-13.51	34.18	17.96	2.648	-14.87
5.25	40.27	17.16	2.773	-19.35	41.76	16.89	2.904	-20.94
5.50	55.24	15.96	2.922	-26.06	55.98	15.40	3.206	-24.97

We also considered fault-free and faulty LNAs at 5.25GHz. For 28 different catastrophic faults, most of the faults are in the lower end of  $V_{T1}$  with varying  $V_{T2}$ . For resistor and transistor

faults, the observed output voltages  $V_{T1}$  remain in far left side as compared to a fault-free value. This result reveals that lower voltages of  $V_{T1}$  indicate faults in resistors and transistors. These results show that the proposed BIST structure is suitable to detect variety of faults. The parametric faults are concentrated near the fault-free case.

Table 3 shows partial list of actual  $V_{T1}$  and  $V_{T2}$  values for several faults of tested results. These results are measured at 5.25GHz. In this table, we considered faults in transistor  $Q_1$  and inductor  $L_b$ . The fault-free LNA provided voltages of 180mV and 445mV for  $V_{T2}$  and  $V_{T1}$ , respectively. These results are used to obtain magnitudes of input impedances, voltage gains, noise figures, and input return losses of the LNA.

Table 3. Measured  $V_{T1}$  and  $V_{T2}$  by BIST.

Test Voltage	$V_{T1}$ [mV]	$V_{T2}$ [mV]
Fault-free	445.0	180.0
$Q_1$ Base Open Fault	127.3	209.6
$Q_1$ B-E Short Fault	127.3	220.0
$Q_1$ E-C Short Fault	155.2	144.6
$L_b + 30\%$	389.3	194.8
$L_b + 40\%$	383.5	192.0
$L_b + 50\%$	375.8	189.8

#### IV. CONCLUSIONS

This paper discussed a new RF built-in self test circuit for measuring RF parameters of 5GHz LNA using mathematical equations and measured DC parameters. The BIST circuit consisted of test amplifier and two RF peak detectors. The test technique using BIST circuit requires only use of common DC meter and RF voltage source generator. Our technique provided significant savings in cost from traditional RF measurements without sacrificing RF values.

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