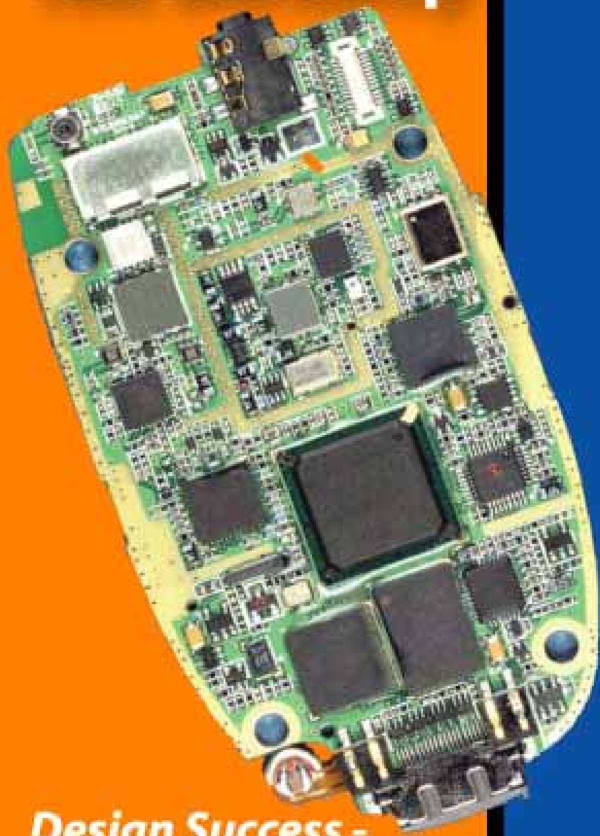
12th Annual
KGD
Packaging &
Test Workshop



*Design Success -
KGD Starts
at the Beginning*

Sept. 11-14, 2005 , Napa, CA

Chip Interface Solution for High Performance SiP

B.Y. KIM

Samsung Electronics Co.

Byeongyun.kim@samsung.com

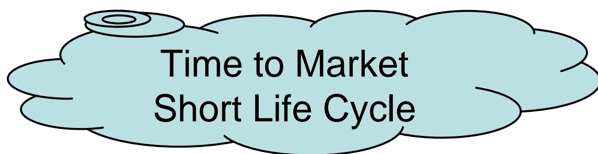
Phone : 82-11-9921-6066

Agenda

- VOC from SiP Biz
- Vop Trend with Technology Node
- Mobile Technology Scaling
- SiP Engineering Barrier
  - Power Delivery Network
  - Interface Engineering
  - Concurrent Simulation Solution
- Cooperation for SiP Enabling

12th Annual
KGD
Packaging & Test Workshop

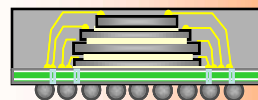
VOC from SiP Biz



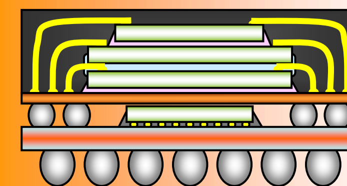
- Higher Density Smaller Geometry
- Mixture of Hetero Chips
- Mixture of Generation
- Higher Performance
- Fast TAT
- Low Cost Solution

Total System Solution in Single Package

MCP

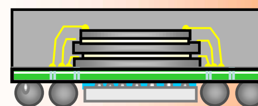


Logic, Memory Stacked

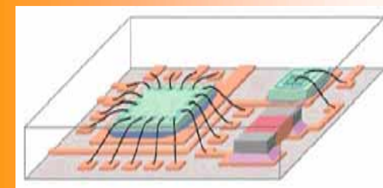


Multi Stack Package

SIP



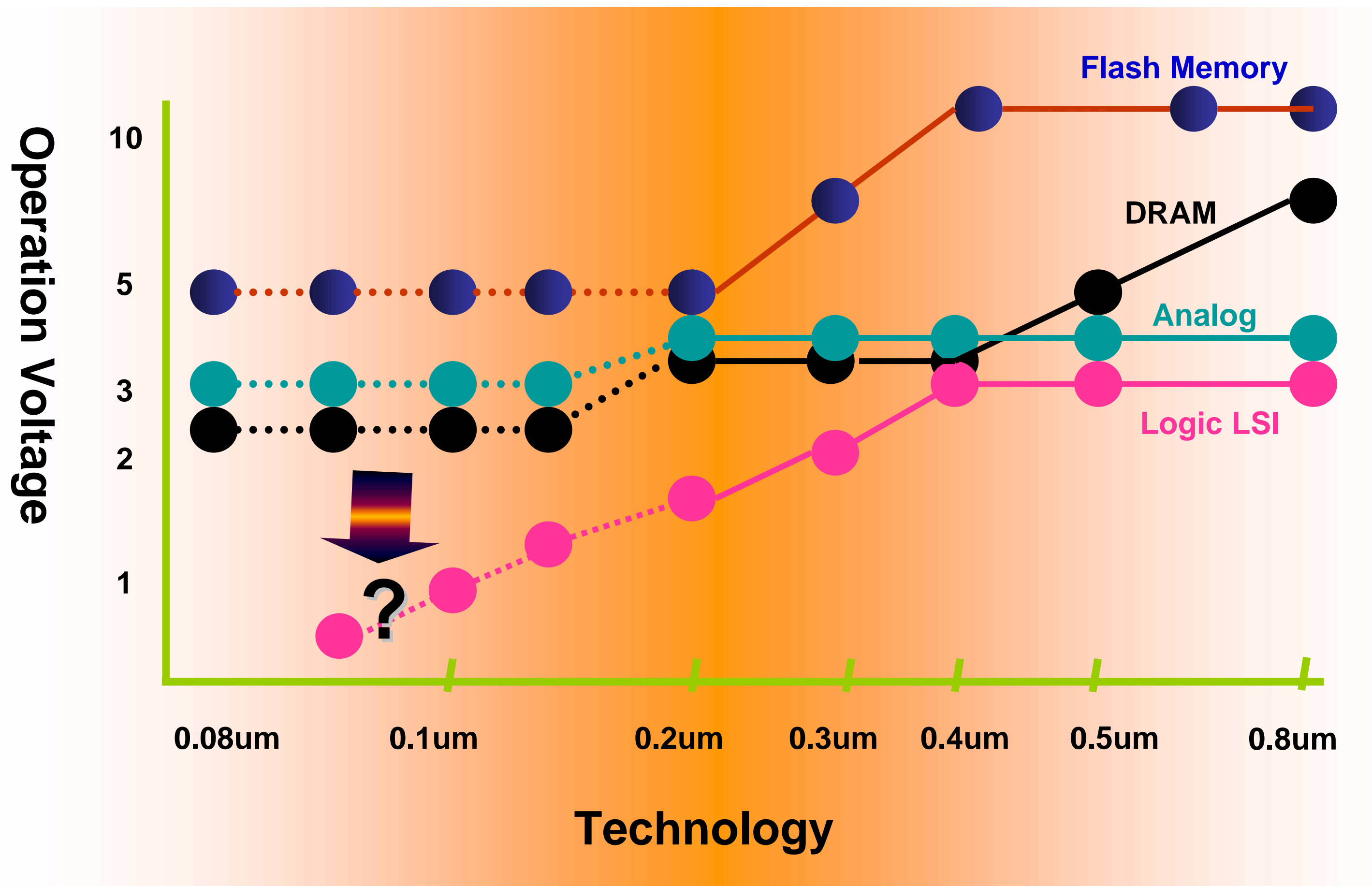
RF, Analog, Passive Embedded



Integrated System Package

Operation Voltage(Vop) Trend with Technology Node

Vop Gap Increase below sub 100nm -> Chip Performance & Immunity ?



Mobile Technology Scaling

Technology Node	0.18um	0.13um	0.09um	0.065um
CPU	200MHz ARM	400MHz ARM	800MHz ARM	1.2GHz ARM
Vop	1.8V	1.5~1.2V	1.1~0.9V	0.9~0.8V
Vthn	<0.50V	<0.40V	<0.30V	<0.25V
PAD Pitch (B)	60um	50um	35um	25um
Off-chip Speed per Pin(Memory)	67Mb /133MB	133Mb /533MB	267Mb /2.1GB	400Mb /3.2GB
Power_Core	2.3	1.8	1.4	1.0
Power_IO (CMOS)	0.85	0.88	1.0	1.0

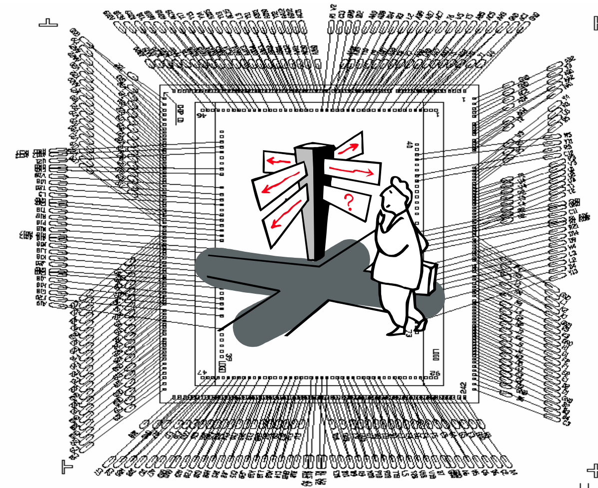
- Power $\propto$ fCV^2, C = Cg + Cn $\propto$ Gate Rule (for Power_Core) or Const (for Power_IO)

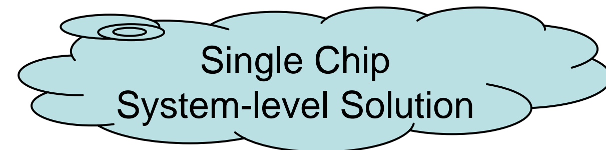
Vth lowering & TR leak increase with Technology Node will provide more chance to lose control in pre-charge circuitry

→ Power_IO to Vth ratio increase 1.7@0.18u to 4.0@0.065u

SiP Engineering Barrier

- ❑ Power Delivery Network
- ❑ Interface Engineering
- ❑ Concurrent Simulation Solution
- ❑ Test & Reliability
- ❑ Thin Wafer Handling
- ❑ On-time Component Validation





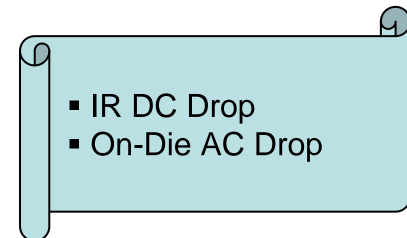
SiP is not a component biz but a system solution service

SiP Power Delivery Network

Goal : Power Delivery without Signal Loss & Reliability Failure

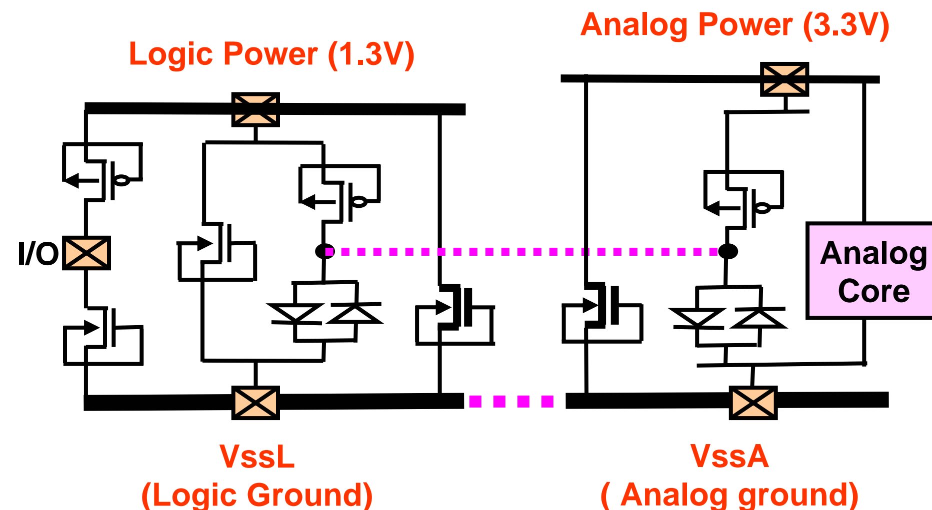
❑ Power Network

- ✓ to deliver a stable power
- ✓ to minimize interference across chips
- ✓ To keep ESD level as good as single component
  - \- Ground Unified or Separate ?
  - \- Parasitic Cap & Mutual Inductance
  - \- Smaller Pad pitch vs L,C increase

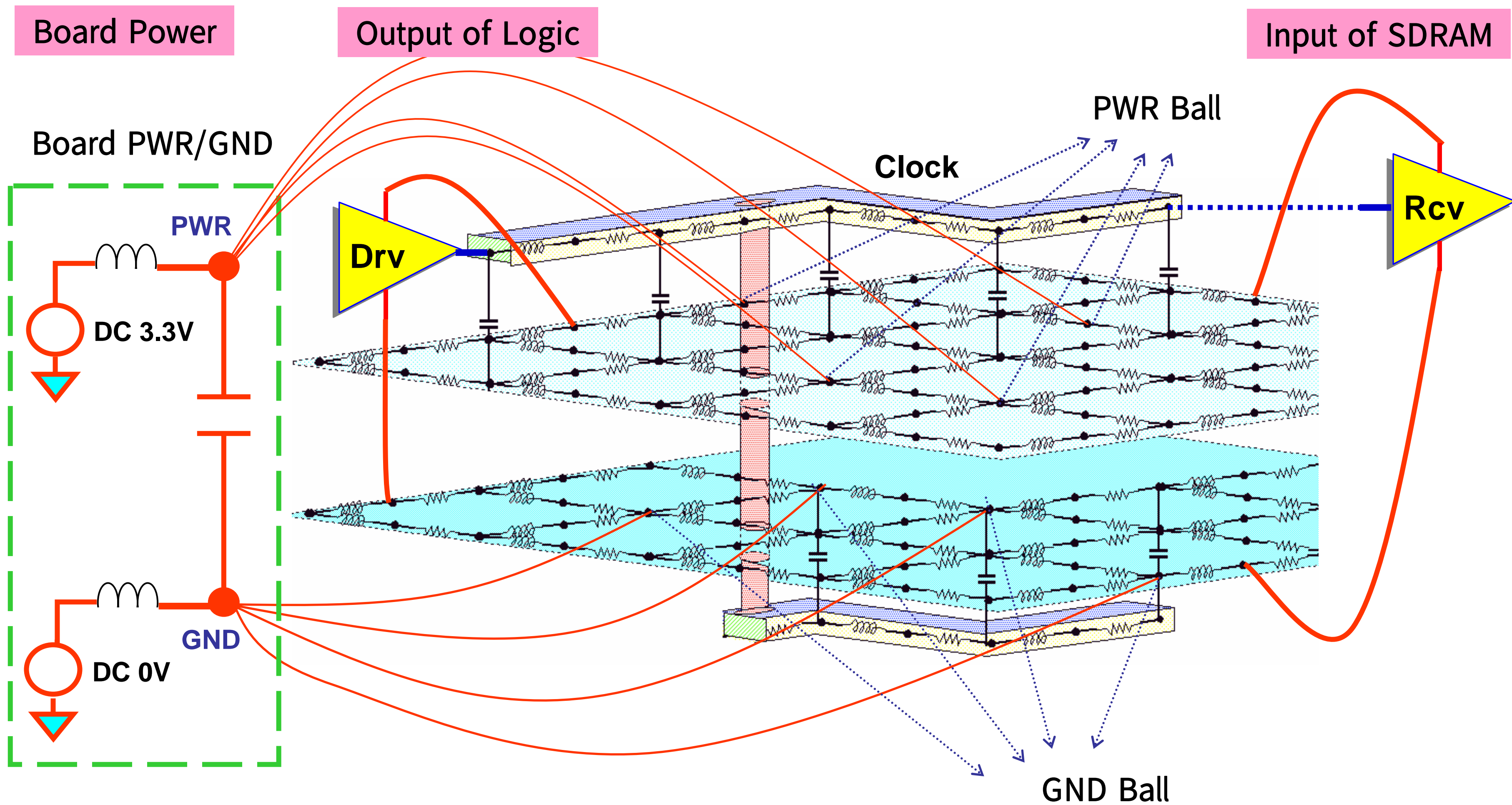


❑ Thermal Problem

- ✓ to explore circuit sensitivity
- ✓ to embed heat detection and control
- ✓ to minimize power consumption
  - \- I/Os, S/A, Clocking, etc

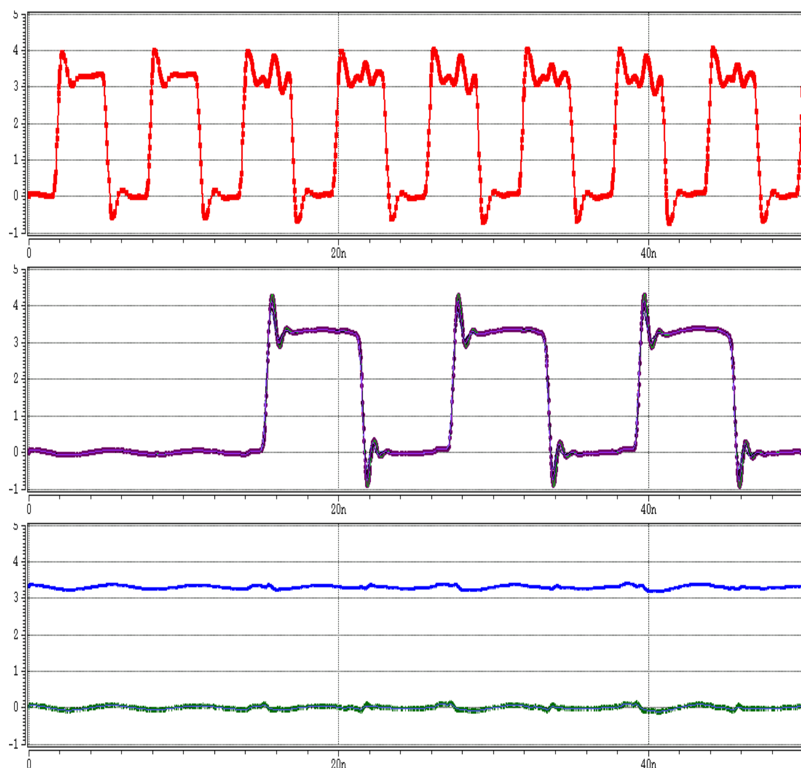


Power Modellng for Interface



Who should be responsible for Board-level Model & Sim… ?

The possibility for potential failure to deliver signals between chip to chip is increasing with SiP, depending PKG + Board design.



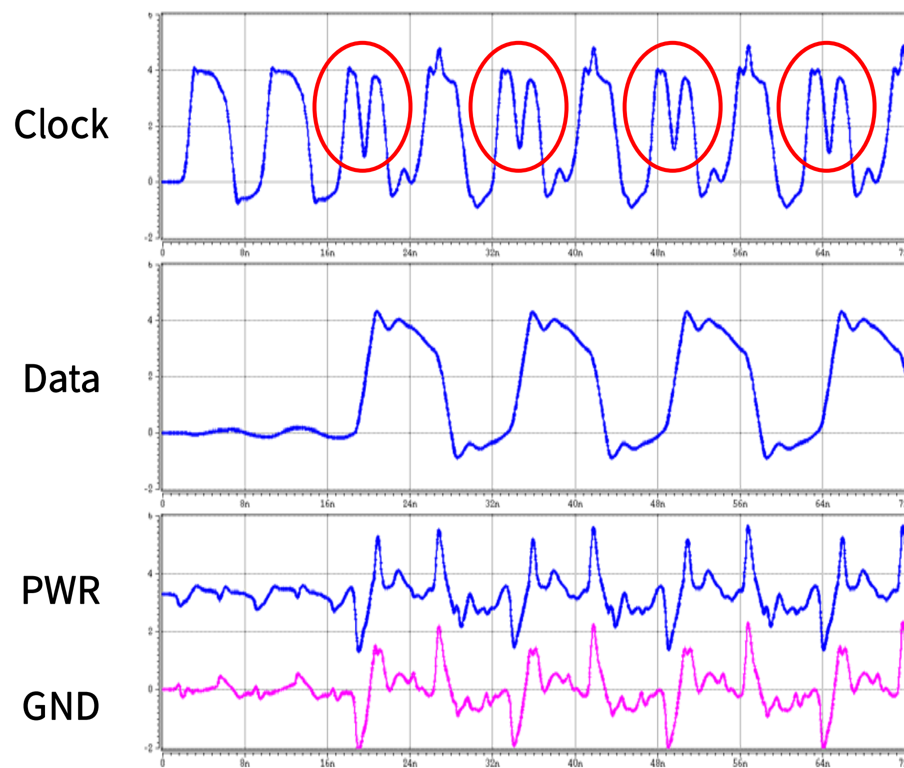
SiP Only

Clock

Data

PWR

GND



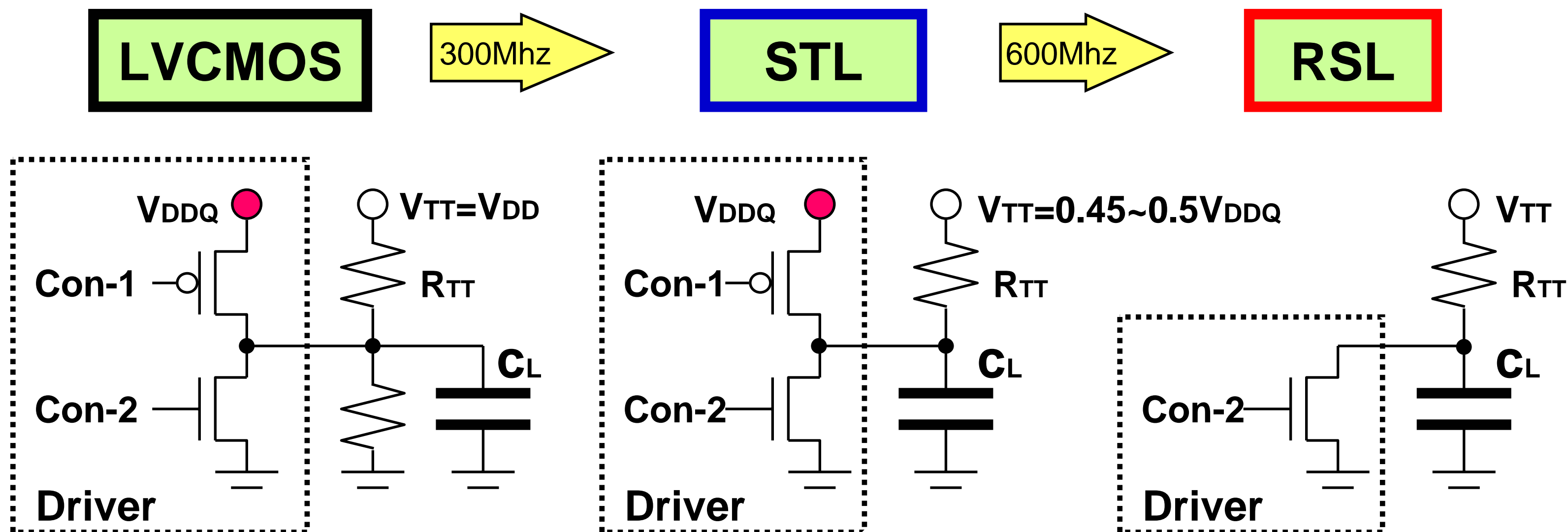
SiP + Board

SiP Interface Engineering

- ❑ Multi-level I/O Structure
  - ✓ Bus, Single-end Topology → P2P, Differential with Termination
  - ✓ LVCMOS → STL, GTL
- ❑ Simultaneous Switching Noise
- ❑ Crosstalk : Inductive (Lm x di/dt), Capacitive (Cm x dv/dt)
- ❑ Signal Integrity : Rise/Fall, Settling, Impedance Matching
- ❑ Coupling Noise
- ❑ Radiation

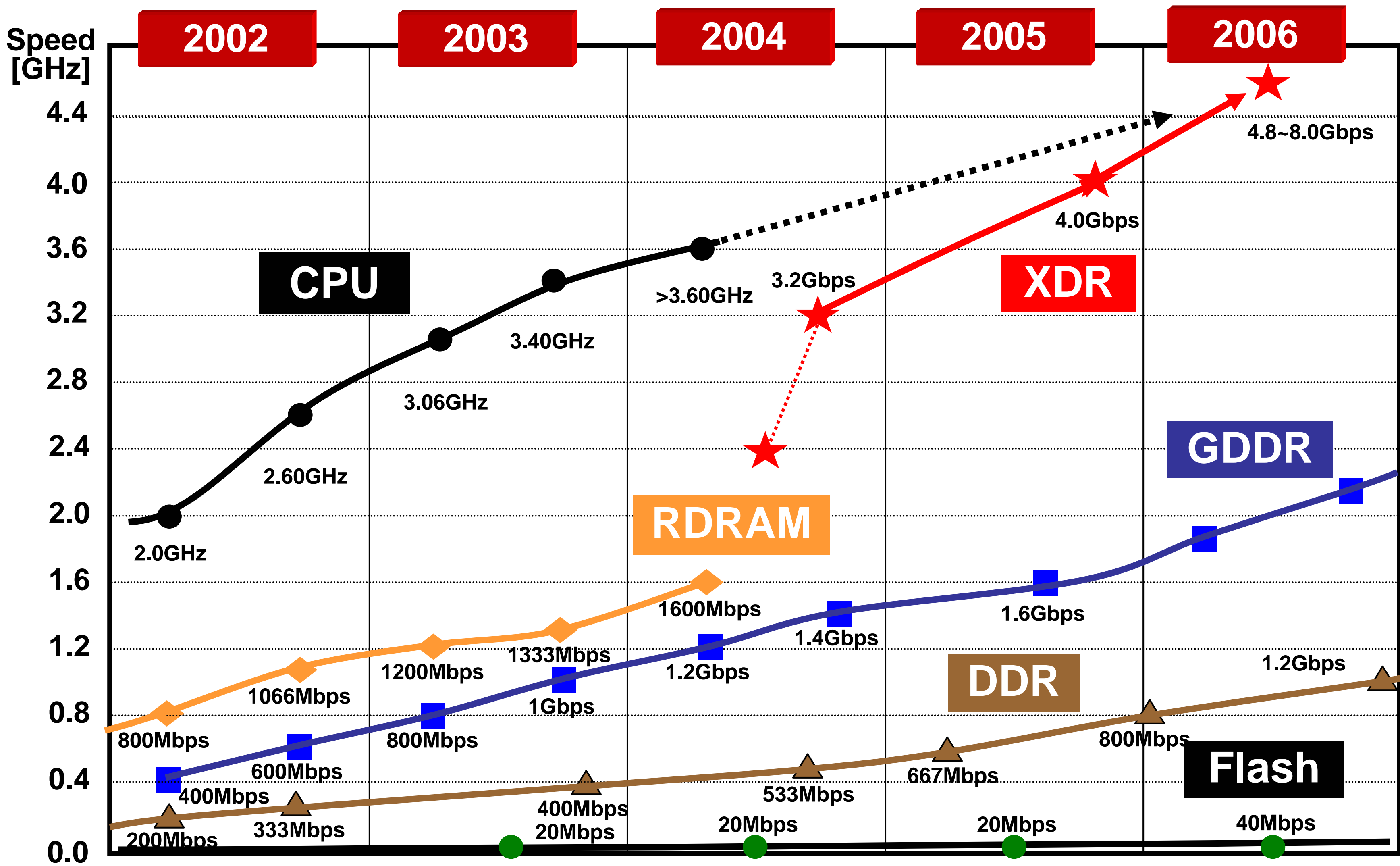
I/O Trasitions for High Peformance DRAMs

- Fast Data Transfer Rate
- Reduced Voltage Swing
- Low Power Consumption



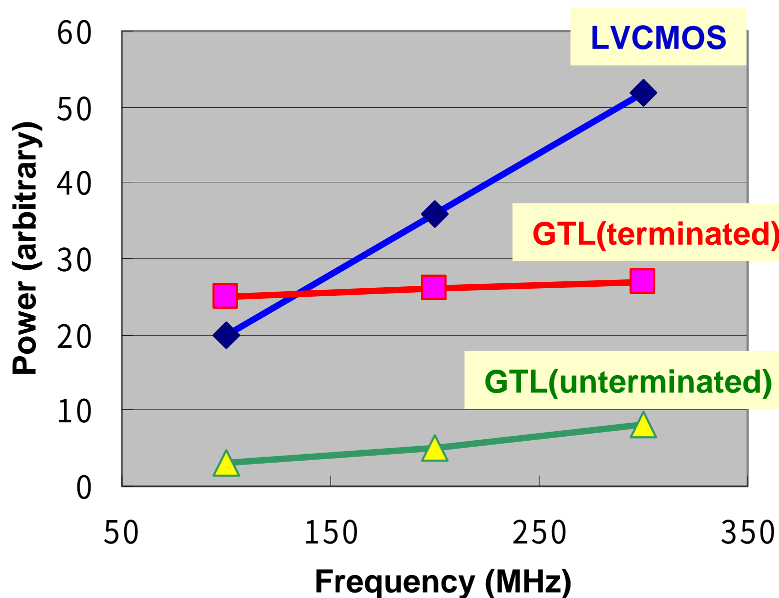
12th Annual KGD Packaging & Test Workshop

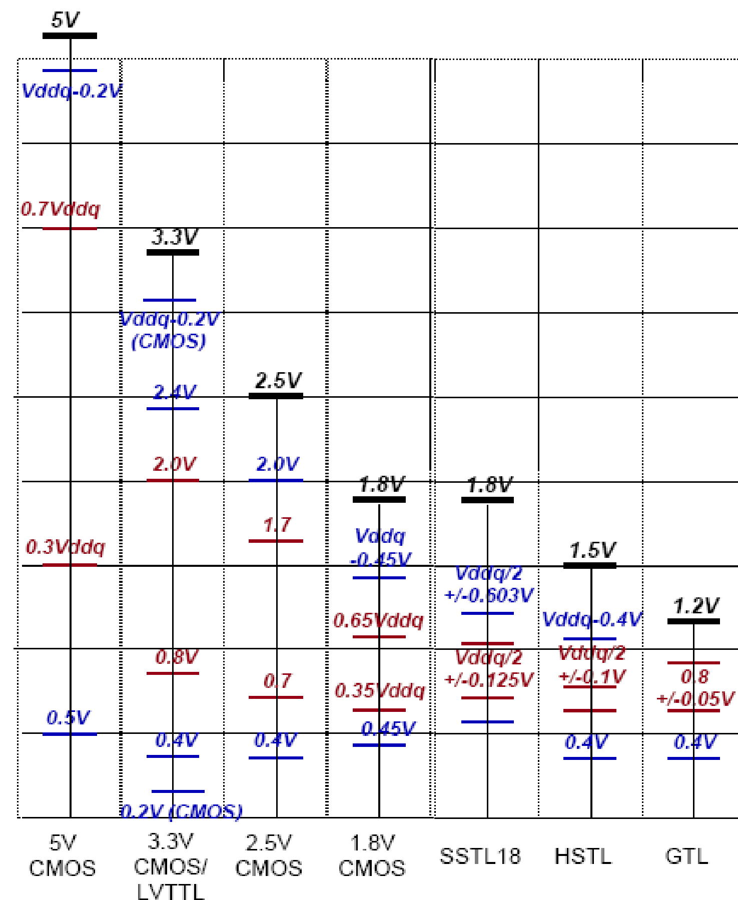
DRAM I/O & CPU Speed Trend



SiP Severity with Multi-level I/O Sharing

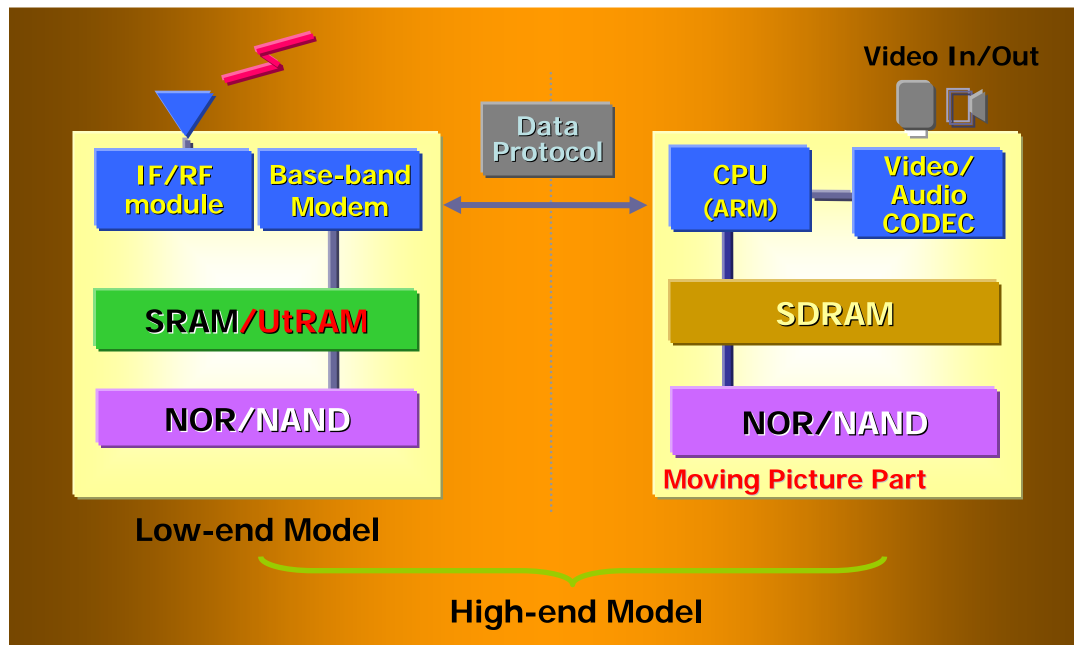
- Bigger Impact than Component
  - ✓ Noise Margin Reduction
  - ✓ Pin to Pin Interference
  - ✓ Chip to Chip Interference





I/O Interface in Mobile System

SSN is not confined inside individual chips but decrease SiP Noise Margin dramatically for small Output Signal Swings in multi-level I/O structure.



DMA Controller

USB Interface
- USB 1.1
- USB 2.0

Card Interface

Memory Controller

- 3.3V LVTTL for SDRAM
- SSTL2 for DDR-SDRAM
- SSTL18 for DDR2-SDRAM
- RTL for RDRAM

Peripherals

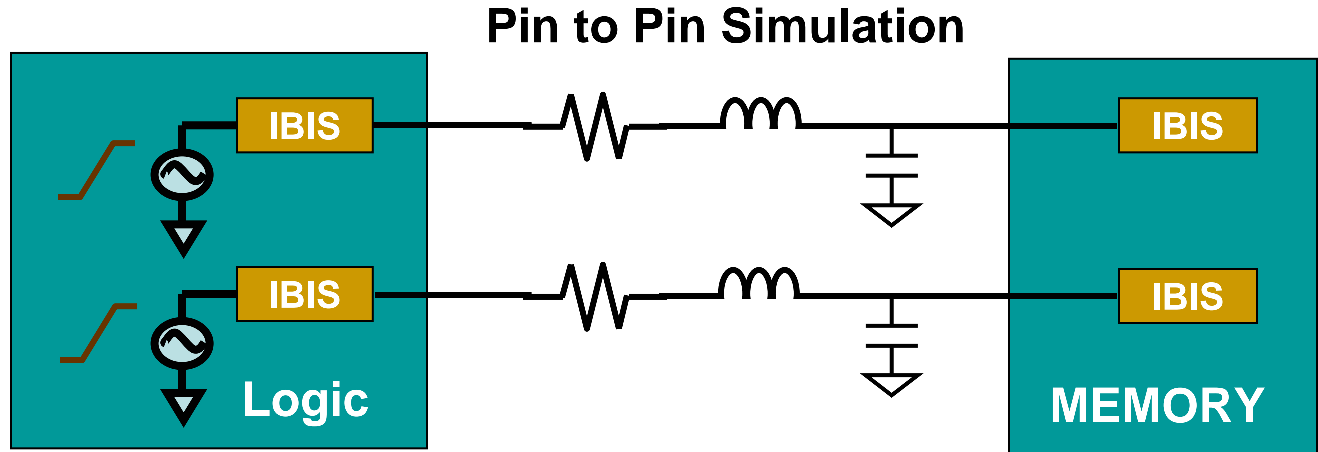
BT, IR, LCD

ATA controller

- ATA100/133
- Serial ATA

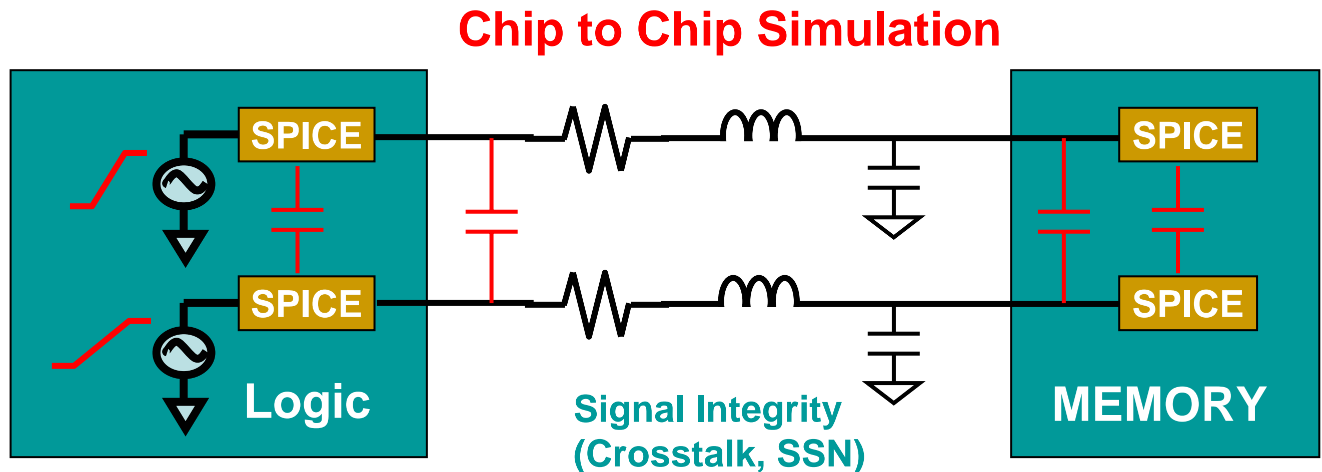
I/O Interface Simulation

Component

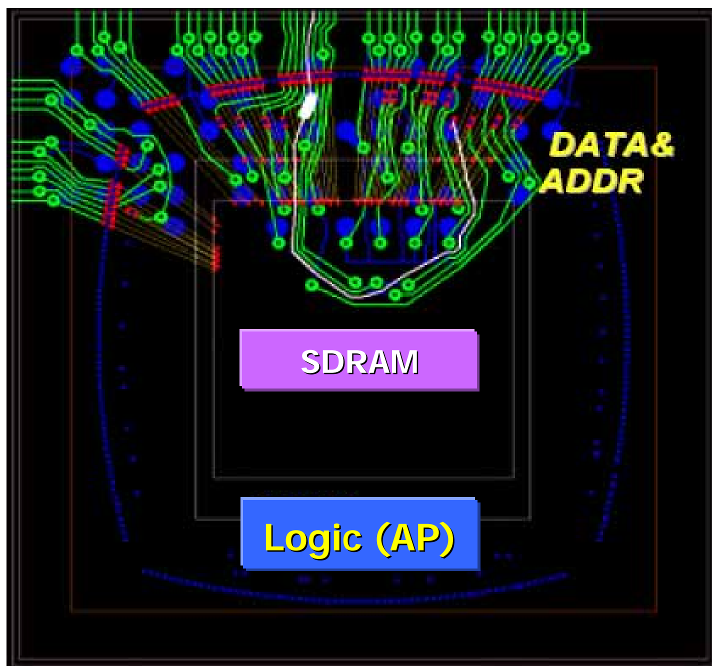


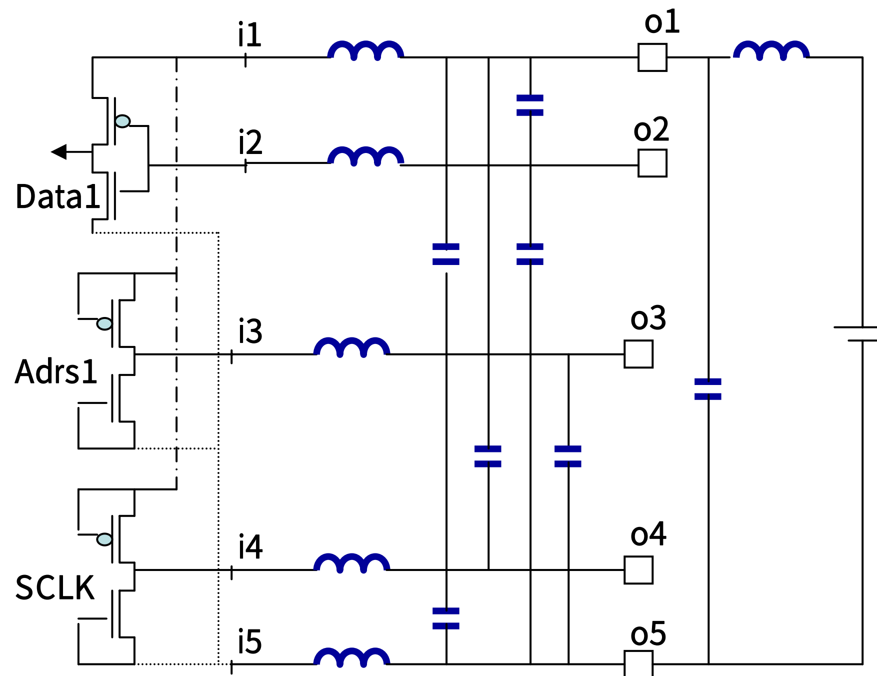
SiP

- Slew Rate Control
- Substrate Coupling
- PCB Coupling



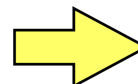
I/O Interface Simulation





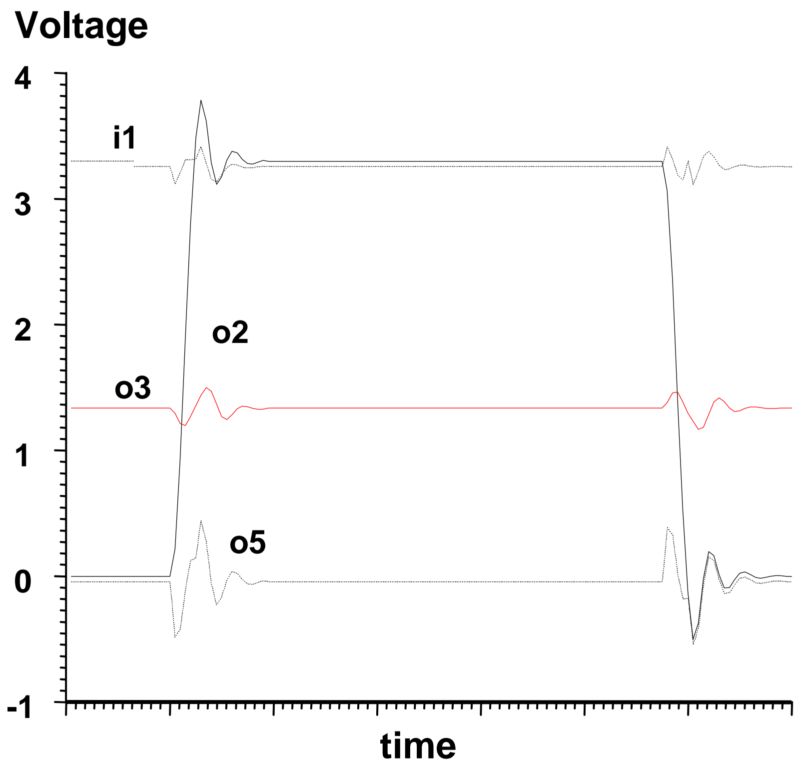
Data Interface
- Slew rate control : 12mA
- Number of I/O : 32

Address Interface
- Slew rate control : 8mA
- Number of I/O : 27



Total Interface
- Number of I/O : 59
- Peak Current : 600mA

I/O Simulation & Measurement



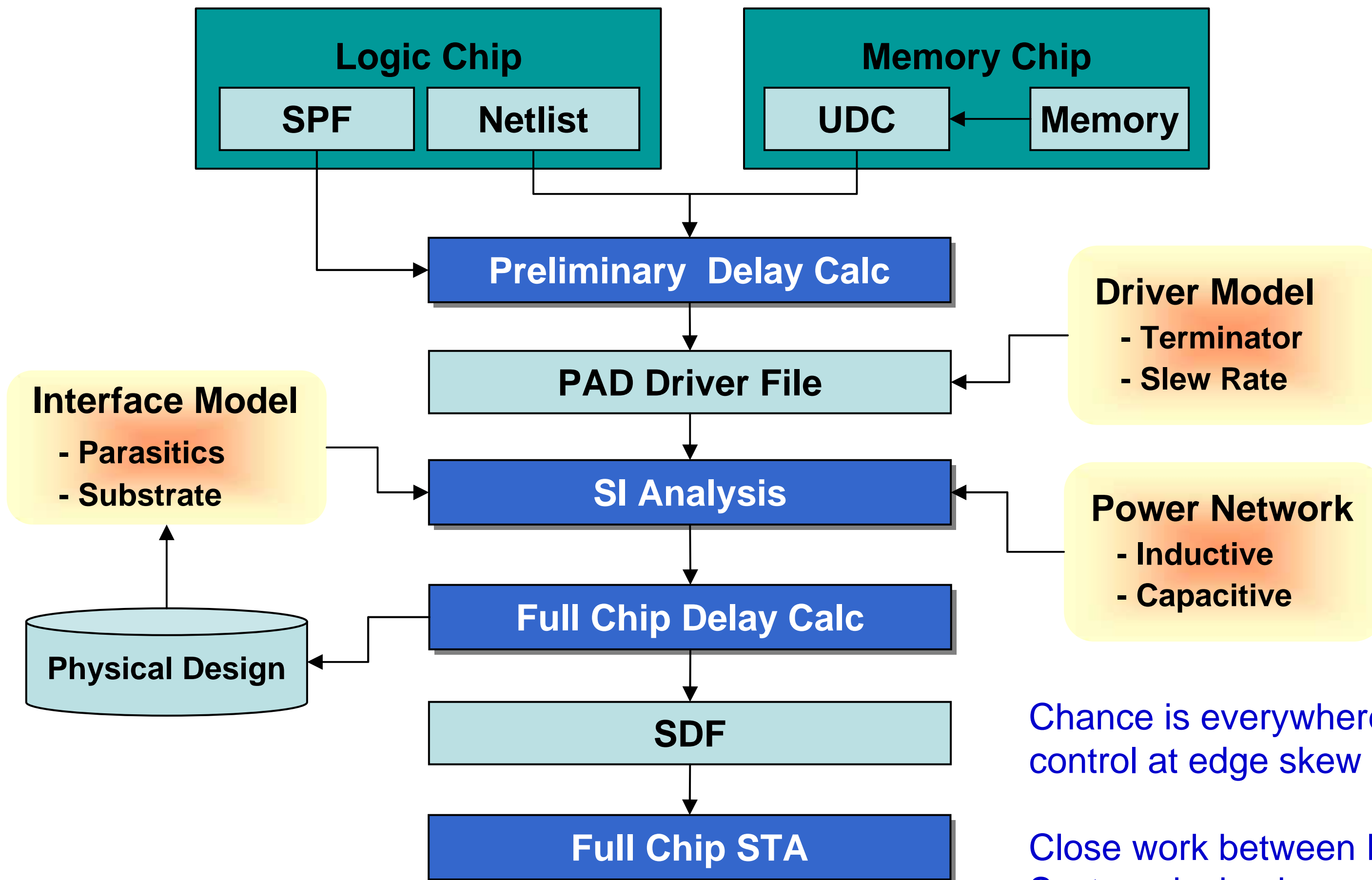
Vdd vs Frq Shmoo

Voltage

Frequency

12th Annual KGD Packaging & Test Workshop

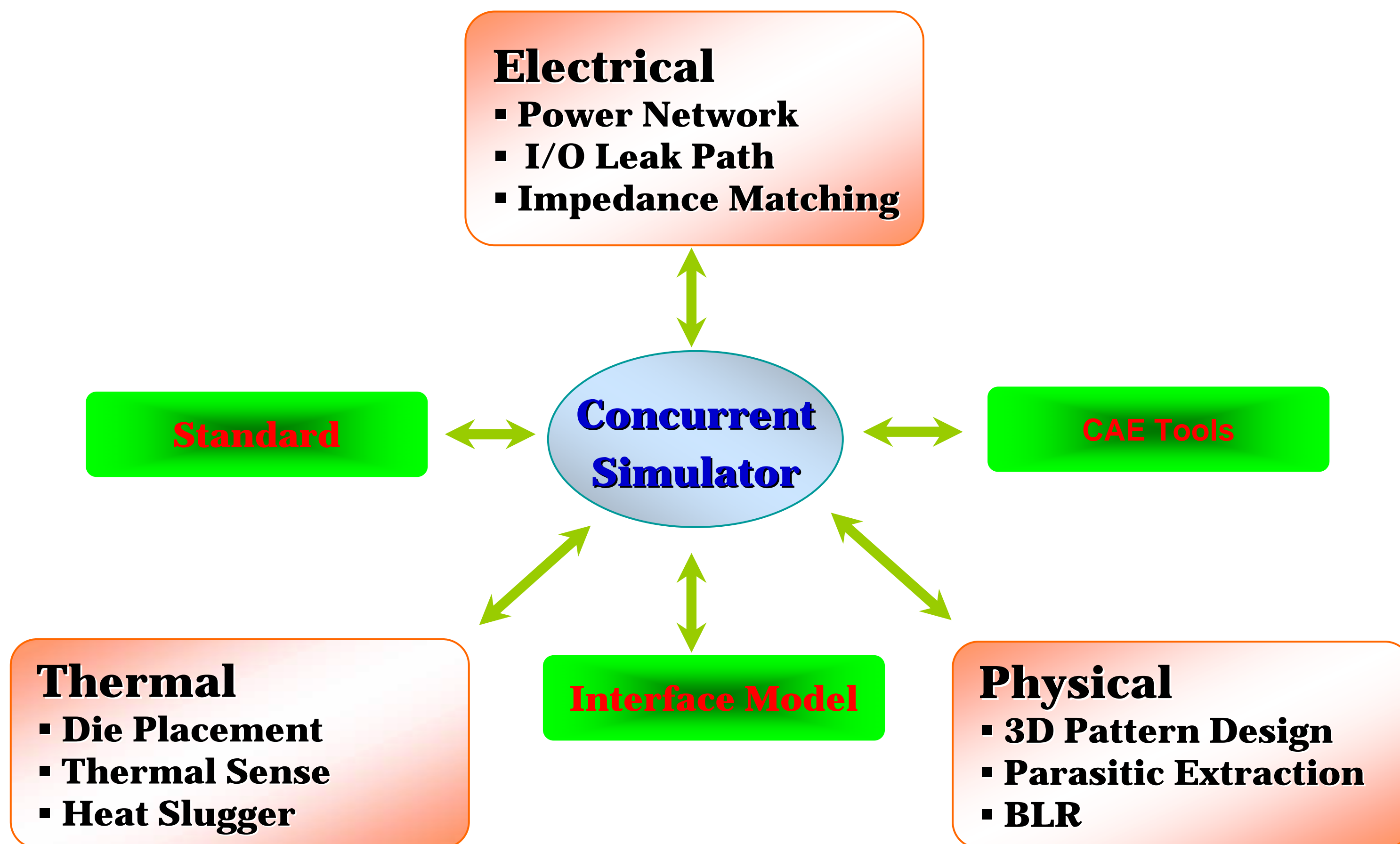
Electrical Interface Design for High Performance SiP



Chance is everywhere my SiP to lose control at edge skew w/o model accuracy.

Close work between Package, Component, System design is very decisive.

Concurrent Simulation Solution



Cooperation for SiP Enabling

- **Co-operation in-between Infra Provider**
  - ✓ to complete seamless Interface model
  - ✓ to prepare user-friendly & re-usable SiP Solution
  - ✓ to co-work with System/Board/Substrate/Component Engineering
- **Standardization between SiP User & Manufacturing Company**
  - ✓ SiP ID designation
  - ✓ Pinmap Information
  - ✓ Z Code control
  - ✓ Thermal Sensor Control
  - ✓ Package Dimension for MSP(Multi-Stack Package)
  - ✓ to unify SiP Terminology

Finally… for Partnership

Thank you.
ありがとうございます.
Grazie.
Gracias.
Xie xie
Danke schön
Merci
Tictac