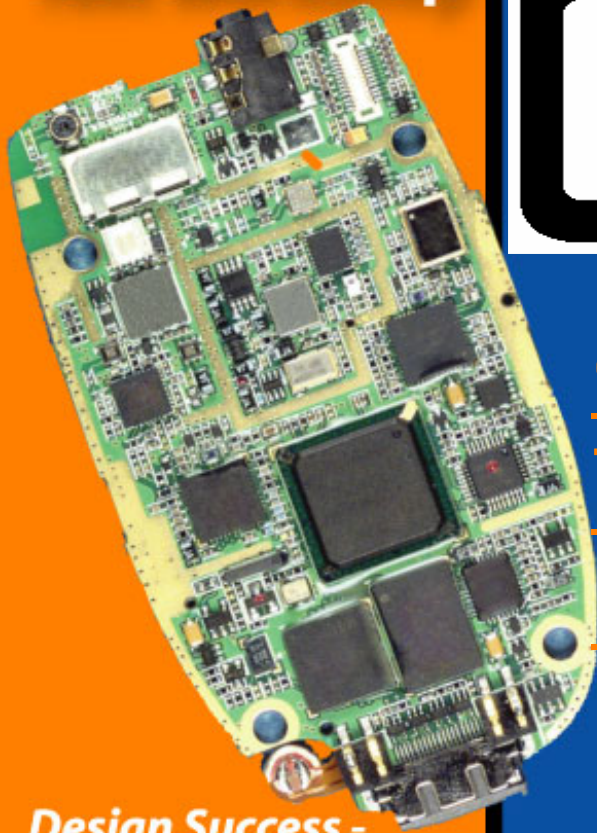


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**KGD**

**Packaging &  
Test Workshop**



*Design Success -  
KGD Starts  
at the Beginning*

Sept. 11-14, 2005 , Napa, CA



**Inapac**

Technology, Inc.

Case Study: A Complete  
Testing Methodology For  
KGD in SiPs

Chiate M. Lin

Corporate Reliability Manager

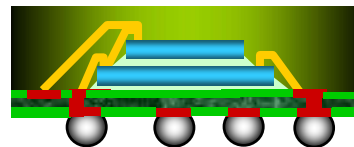
Inapac Technologies, Inc.

# Inapac Technology Inc.



Inapac Provides Innovative Intellectual Property, Methodology and Services for Reliable **System In Package** (SiP) solutions

- ▶ Initial I.P. products include memory designs optimized for SiP
- ▶ Supported I.P. business model includes services to support methodology



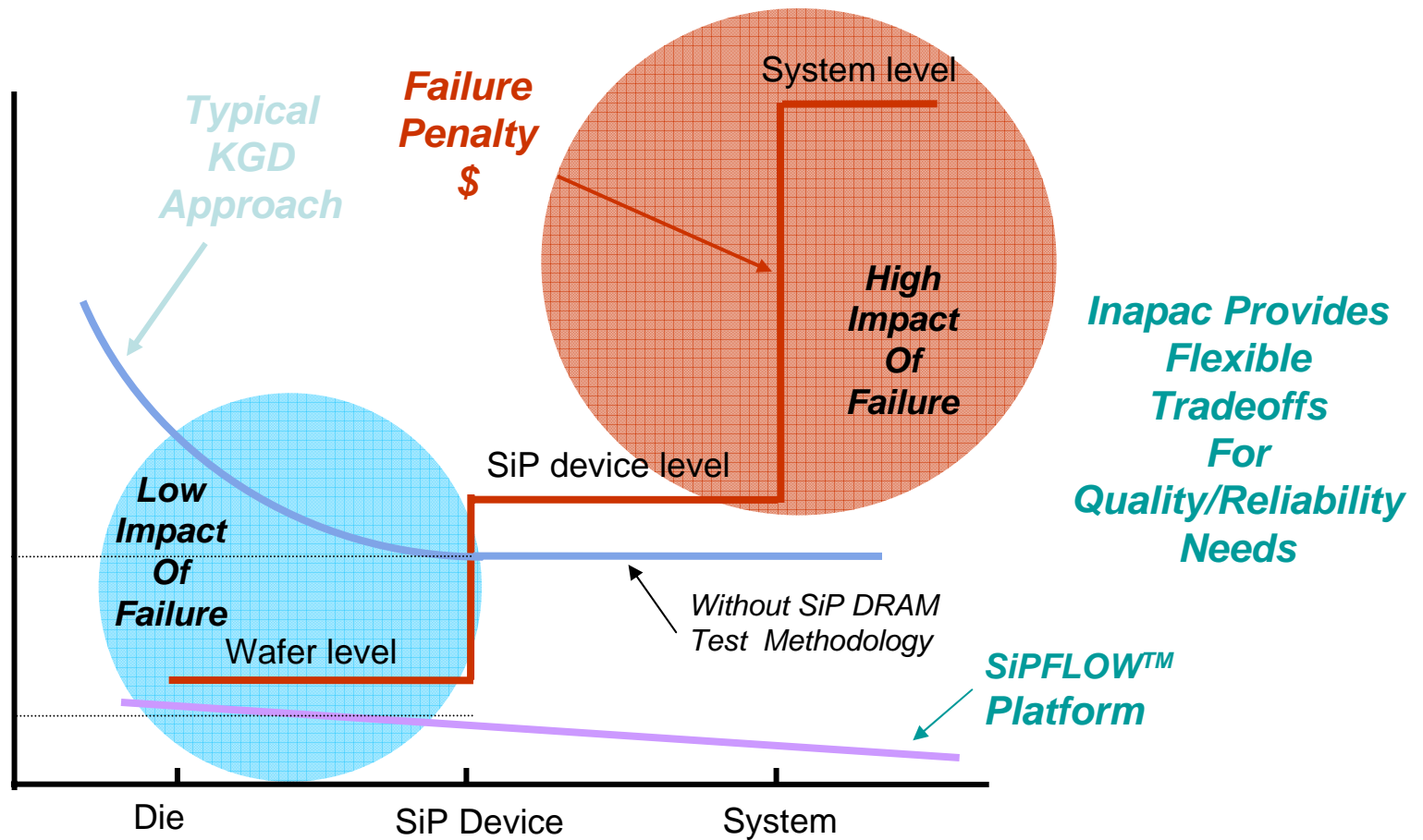
Sept. 12-15, 2005

Napa, California

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# Has Your Known Good Die Died?

## Reliability Impact



1000  
dppm

200  
dppm

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# Inapac Mission Overview



- Solve the biggest hurdle in integrating DRAM into SiP.
  - No package level burn-in (**VIBETM**)
  - Meets and exceeds customer quality and reliability expectations (**SiPFLOWTM**)
  - Low cost/high throughput DRAM FT (**SiPLINKTM**)
- Turnkey DRAM solution for your SiP memory requirement (**SiPFLOW Platform**)
  - Design support
  - PE and TE support
  - FA support



## V.I.B.E.<sup>TE</sup> (Voltage Burn-in Emulation)

- Replace traditional DRAM 'burn-in' with more effective approach for SiP
- Traditional burn-in aims at accelerating failures through temperature and voltage stress
- Voltage is a more potent acceleration factor if applied properly
- Similar Quality to traditional post burn-in can be reached through voltage stress in a much shorter time

# VIBE Results Presented last year



129 DPM, 5 Fit @ 60 C.L.

## Post V.I.B.E. Qualification Results (Foundry B):

Test Item	Test Condition	Sample Size	Stress Hours	DPM, 60% CL	DPM, 90% CL	Gamma used
ELFR	Ta=125°C, Vcc=4.1V	10,239/2*	24 hrs**	129	220	3.4
*1 Idd failure						
*1 Bank0 failure						
** See appendix for DPM calculation of other ELFR test durations						
Test Item	Test Condition	Sample Size	Stress Hours	FIT, 60% CL	FIT, 90% CL	Gamma used
HTOL	Ta=125°C, Vcc=3.9V	231/0	1000 hours	5	11	3.4
Activation energy- 0.7ev, Lambda= 0.6						
Use Temperature- 50°C Ta = 114°C						
Temperature at Stress conditions- 125°C						
Use Voltage- 3.3V						
Stress Voltage- 4.1V for ELFR Va = 14.8 (ELFR)						
3.9V for HTOL Va = 7.8 (HTOL)						
Gamma = 6 but derated to 3.4 in this calculation for margin						

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# 16M SDRAM Quality and Reliability Status



- **Stand alone Memory**  
– *>6.5M pieces produced*

Early Life Failure Rate (ELFR)	129 DPPM
Long Term Reliability Failure Rate	5 FIT
Ongoing Reliability Monitor Program	Ongoing (0 FIT)
Outgoing Quality	0 PPM

# 16M SDRAM Quality and Reliability Status



- **Logic- Memory Integration (SiP)**
  - *>1.5M pieces through Final Test*

Electrical Outgoing Inspection	1* (test escape, coverage added)
Warranty Returns	None
Field Returns	None
RMA Requests	None

# 16M SDRAM Quality and Reliability Status



- **End Customer (Mobile Phone- final assembly)**

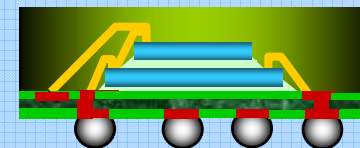
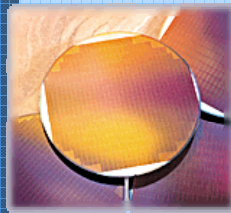
Electrical Incoming Inspection	No reported Memory rejects
Warranty Returns	None
Field Returns	None
RMA Requests	1*(unconfirmed)

# SiPFLOW™



## SiPFLOW Methodology

SiPFlow Enabled  
Memory Device



Better quality  
Better reliability  
Memory die

SiP  
(ASIC + DRAM)

High quality  
High reliability  
SiP

### Wafer Level Tests

- VIBE Wafer Level Test
- Proprietary Screen Tests

SiP Product  
Lifecycle Test Cost  
Optimization

### Package Level Tests

- SiPLINK Gateway
- Full Access Final Test

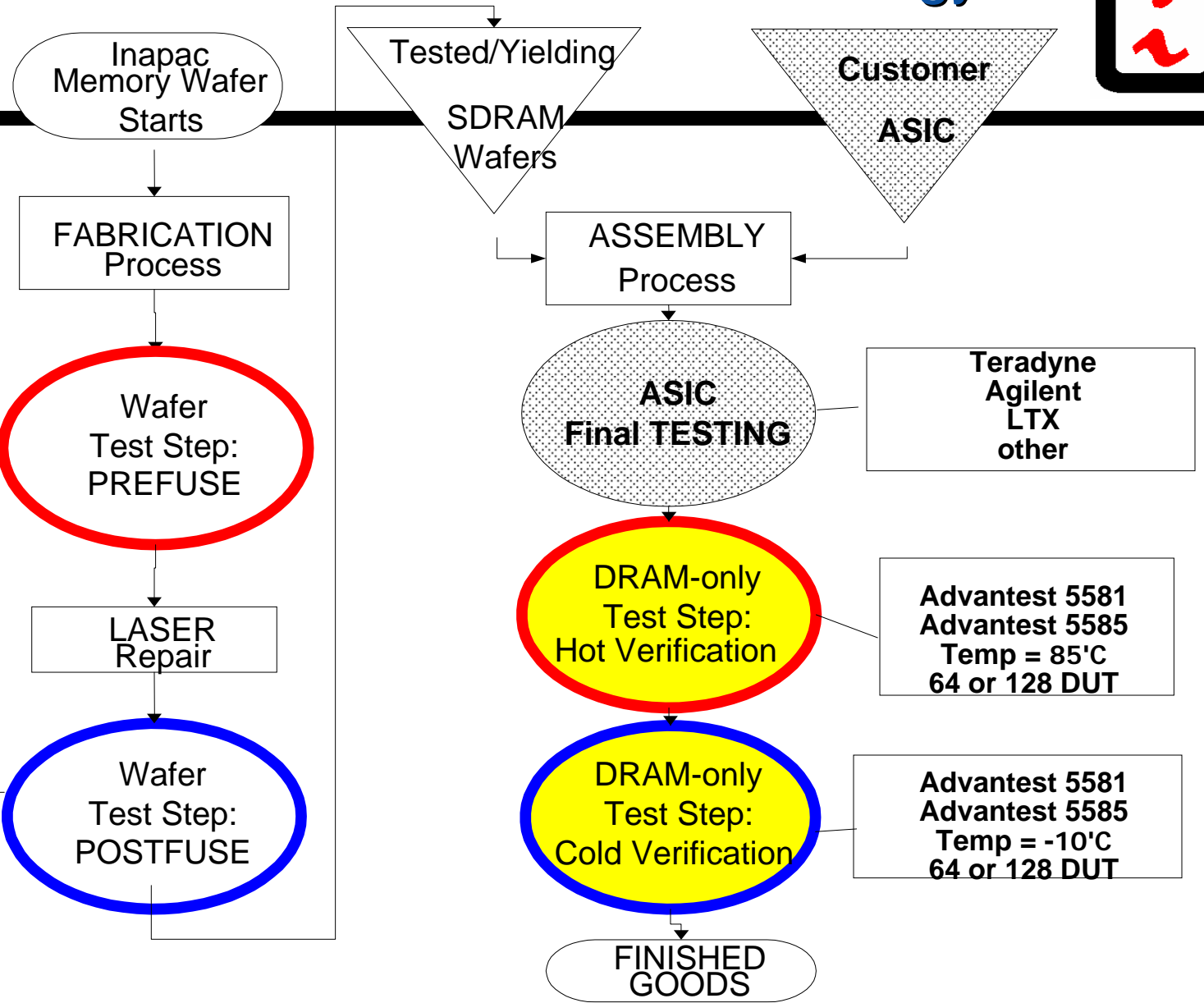
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**Infrastructure For Maximizing SiP Yield & Reliability at Low Cost**

# How to achieve these exceptional numbers with SiPFLOW Methodology



Advantest 5335P  
 Temp = 85°C  
 32 or 64 Device Prob

Advantest 5335P  
 Temp = 25°C  
 32 or 64 Device Prob

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Packaging &  
Test Workshop

**SiPLINK™**



- Programmable test controller
  - control test modes, test sequences, and memory access
  - generate specific test patterns
- Massively parallel internal test path
- Set of precision analog voltage pins
- Control and data pins
- Proprietary algorithms embodied in wafer and package test programs

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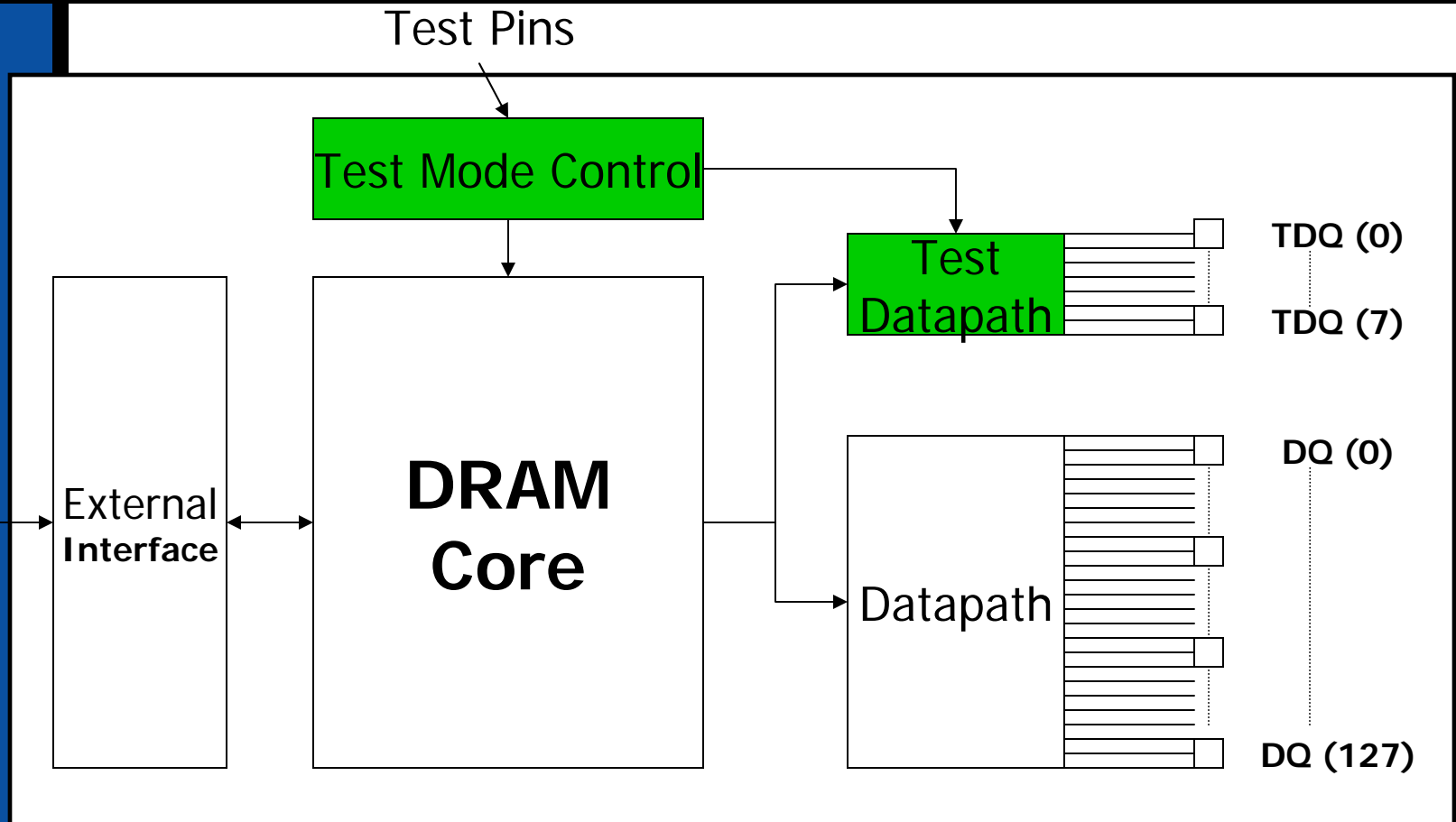
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# SiPLINK Gateway In A Nutshell

ASIC



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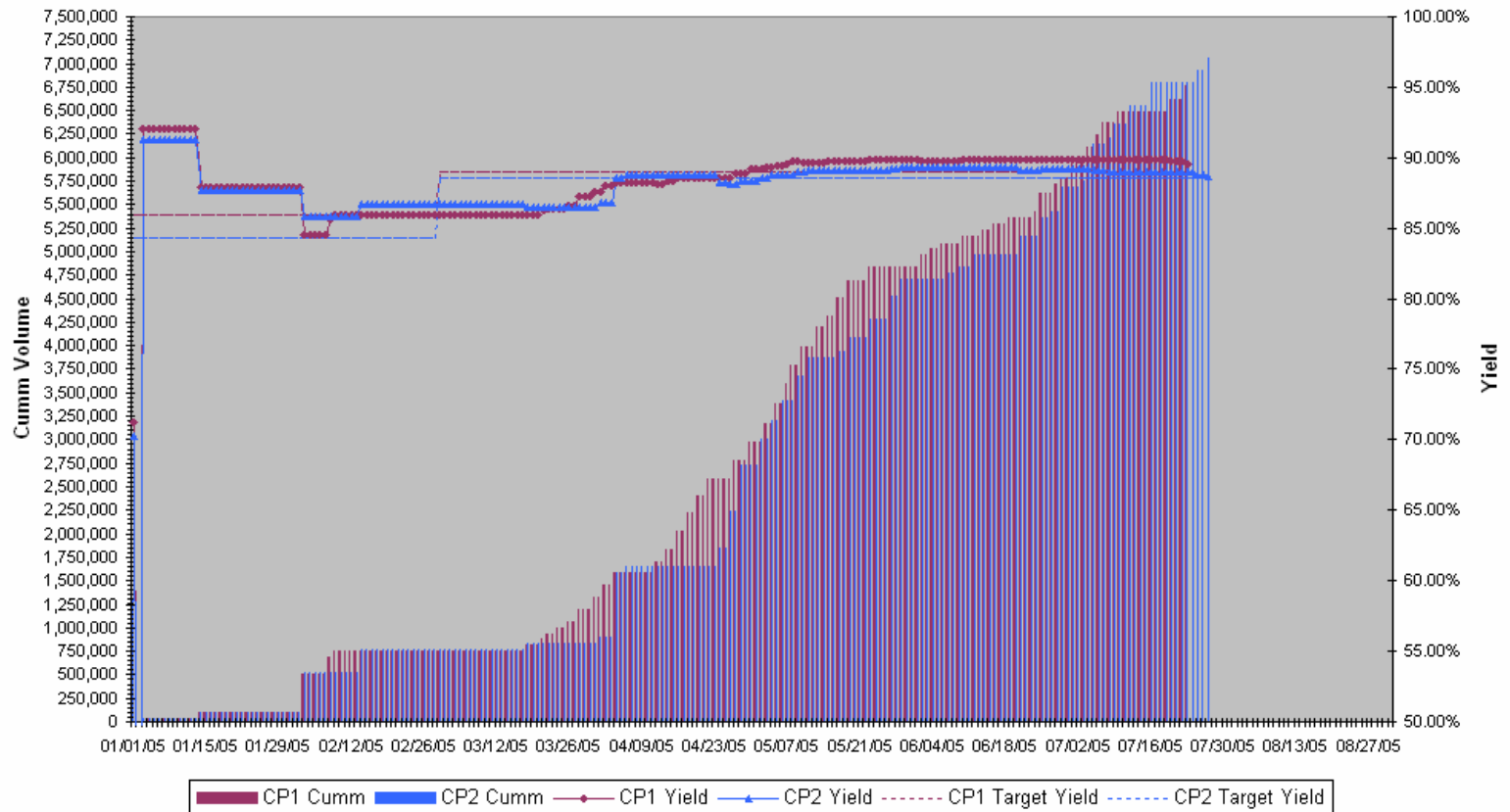
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Separate Test Path Enables Reduced-Pin Testing

# Actual cumulative CP Yield Data

CP1/CP2 Trend



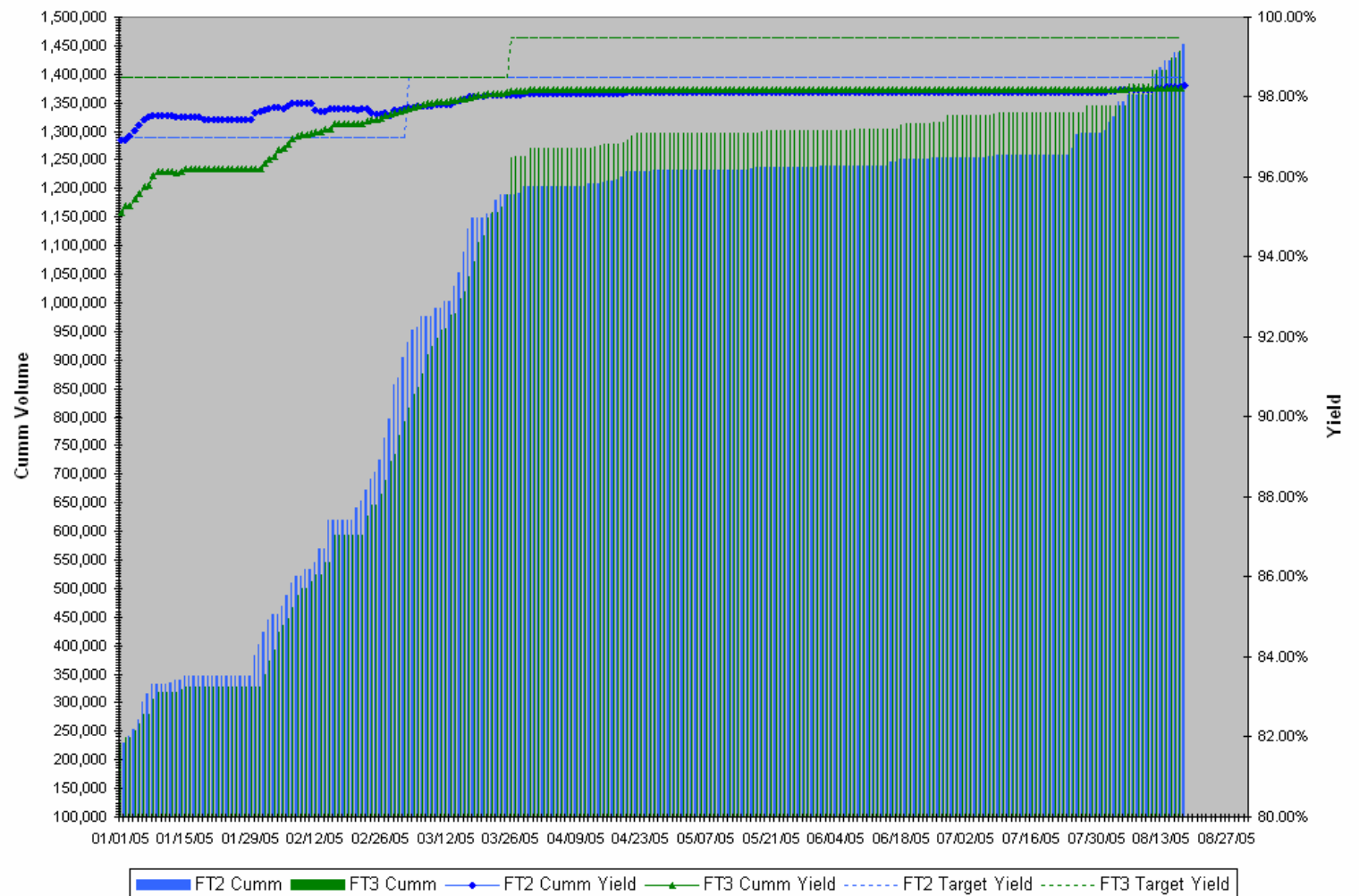
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# Actual cumulative FT Yield Data

FT2/FT3 Trend



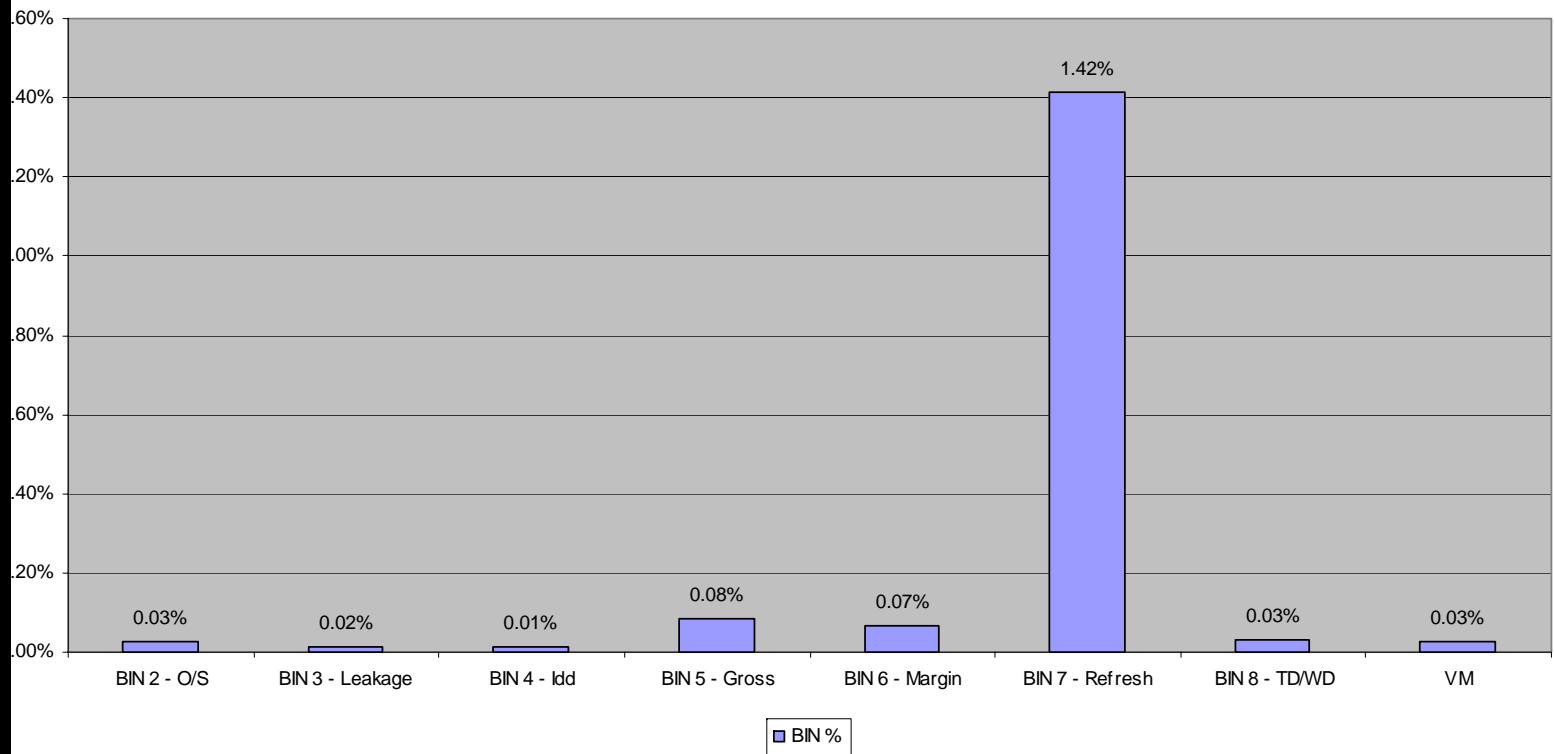
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# Actual cumulative FT2 Bin Data

FT2 Fallout Pareto



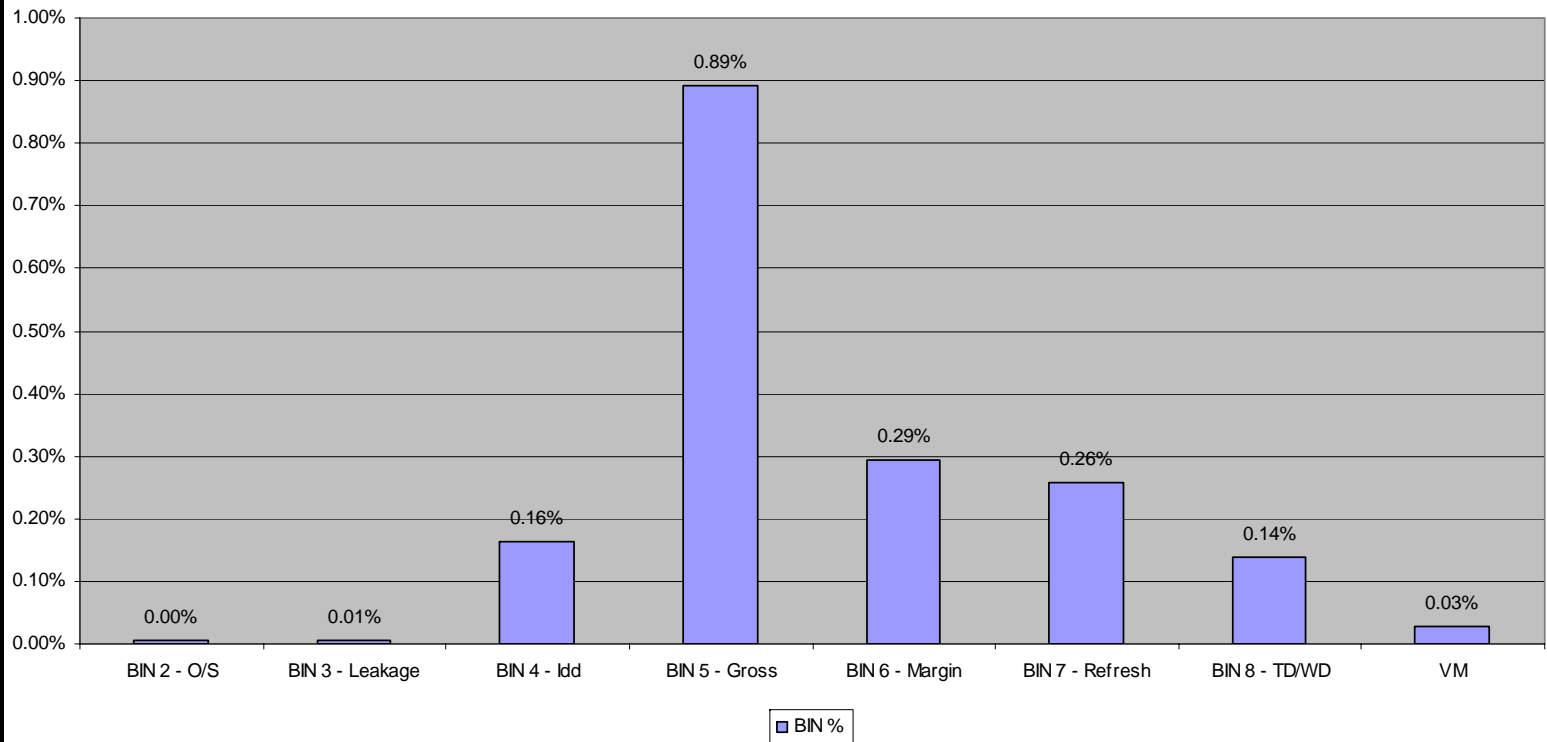
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# Actual cumulative FT3 Bin Data

FT3 Fallout Pareto



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# SiPFLOW Platform Deliverables



## Inapac Design Services

SiP Package Design Services

Customized Test Reduction

Failure Analysis

Yield/reliability monitoring

## Inapac Test System

Wafer Sort (CP) Test S/W

SiP Device (FT) Test S/W

Wafer Probe Hardware

Load board Hardware

## Inapac Silicon IP

SiP optimal bond pad organization

SiP Optimized Memory Designs

VIBE Circuits

SiPLINK Logic

## Technology Node

Memory Cell/Array

Process Geometry

Foundry

Memory Type

*Inapac Unique Value*

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# Conclusion

- SiPFLOW platform that goes beyond KGD to deliver high quality and reliability at low cost
  - ▶ Optimized tradeoffs between wafer sort and SiP level tests
  - ▶ SiPFLOW methodology is a technical and economic reality
- Cost-effective product strategy and support for high volume production
  - ▶ SiP optimized DRAM designs
  - ▶ Direct foundry purchase model
  - ▶ Customized services to lower costs over product lifecycle
- Only Inapac offers SiPLINK test gateway capability
  - ▶ Test procedure to ensure un-compromised reliability
  - ▶ No dedicated test pins (Patented Approach Granted)