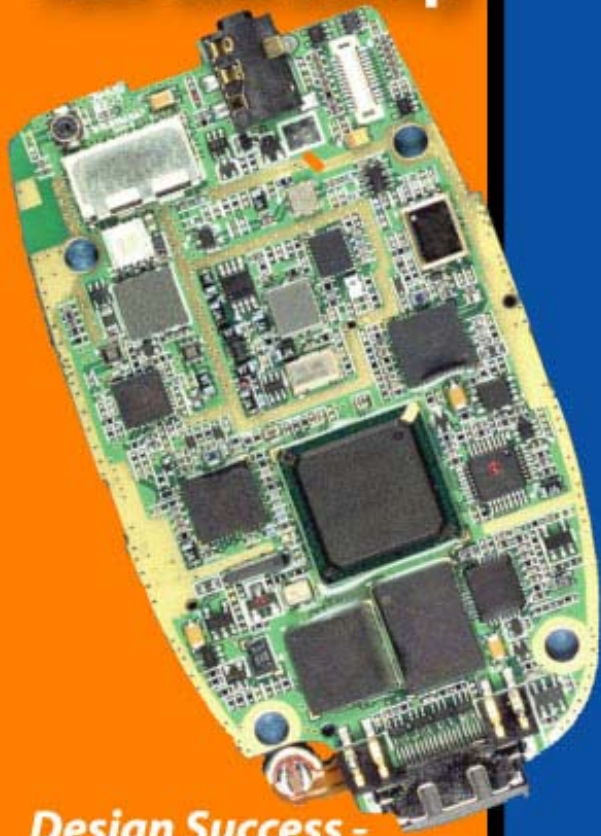


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Sept. 11-14, 2005 , Napa, CA

DRAM Design for KGD

The “2T” Architecture

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Introduction

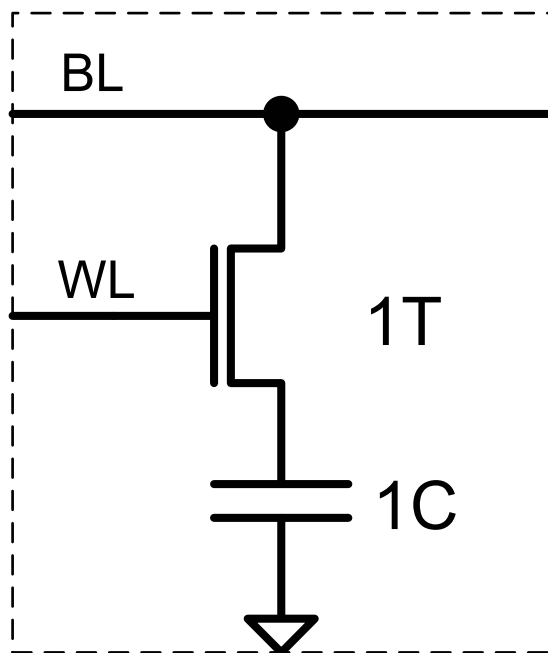
- Due to the inherent “analog” nature of DRAM, test times are typically an order of magnitude longer (or more) than logic devices.
- Historically, DRAM has required multiple hours of burn-in stress.
- At lower DRAM densities, KGD test costs can approach die cost.

Introduction

- Most DRAM KGD efforts are focused on acceleration techniques and data compression to efficiently and cost-effectively test die-level products.
- Micron has demonstrated through architectural design techniques that the amount of KGD test can be reduced, and extended burn-in eliminated, while providing high quality and reliability levels.

Technical Overview

- Mainstream DRAM technologies utilize a 1-transistor/1-capacitor (1T/1C) architecture as the unit cell.

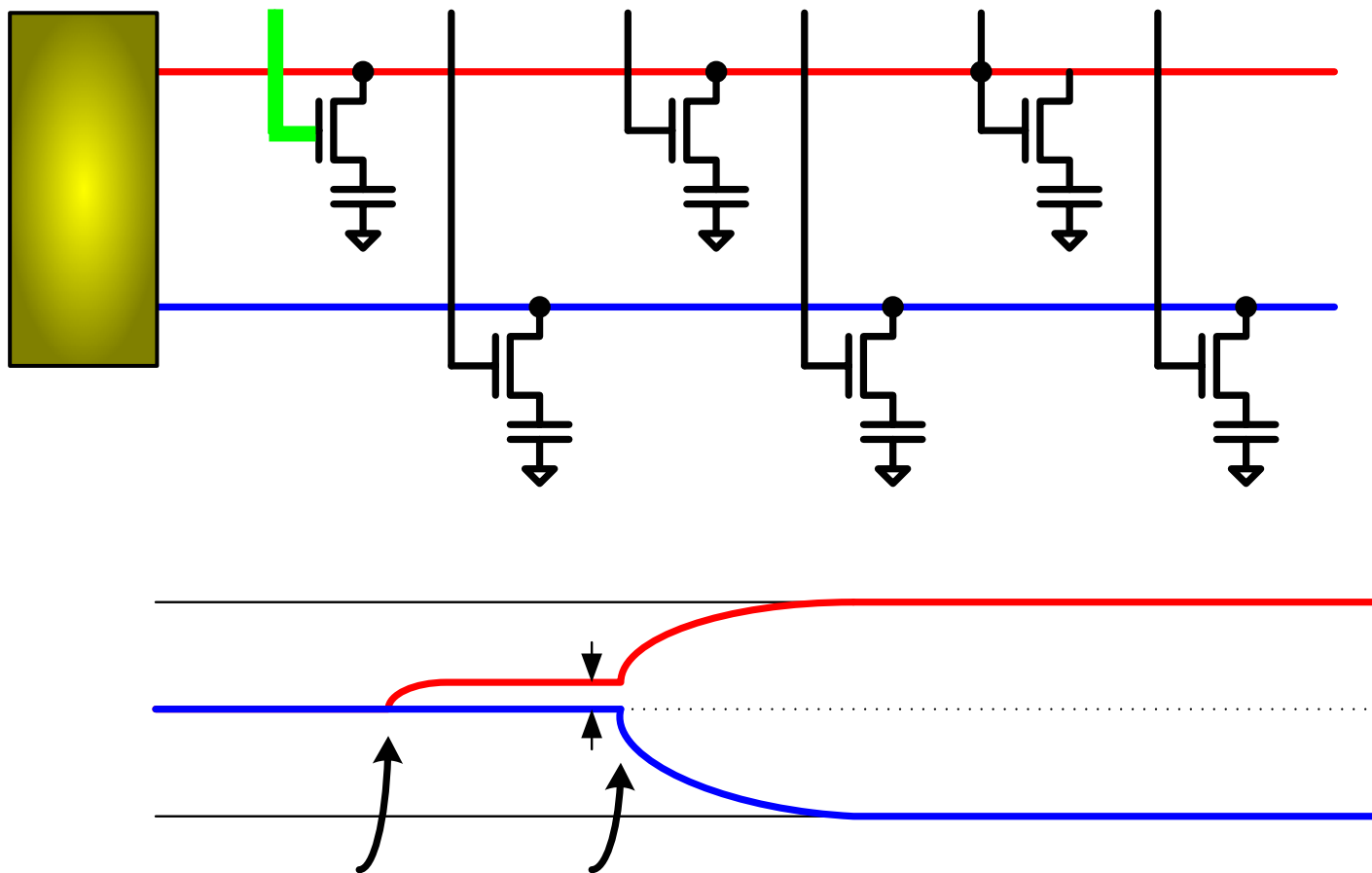


Note:

BL – Bitline

WL – Wordline

Mainstream “1T/1C” Architecture



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The “2T” Architecture

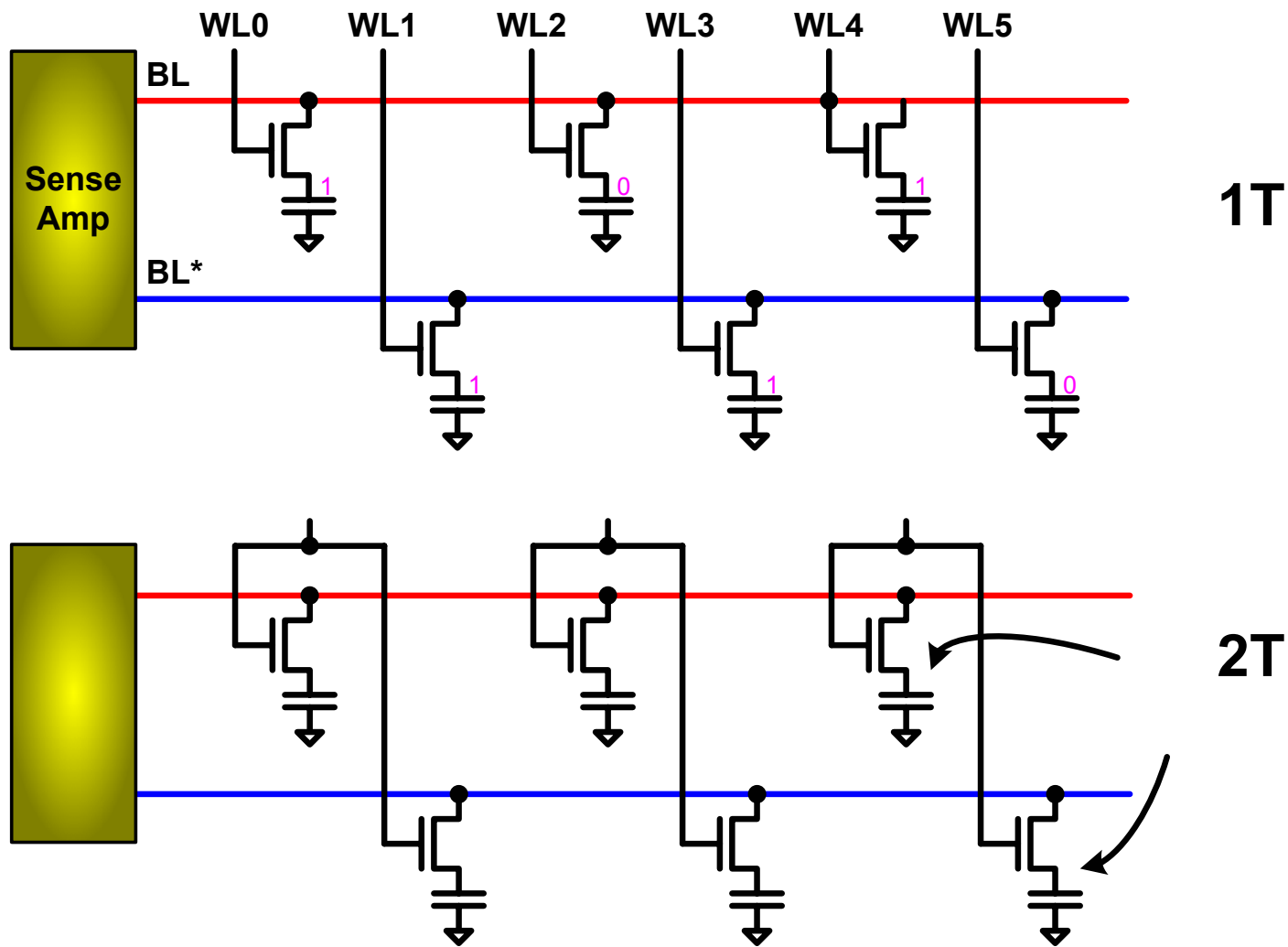
- Actually “2T/2C” but called “2T” for brevity
- Effectively uses two unit cells to comprise one logical “super-cell”
- Easy to implement with existing cell layouts by eliminating wordline decoder LSB term or physically shorting adjacent wordlines

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“1T” vs “2T”

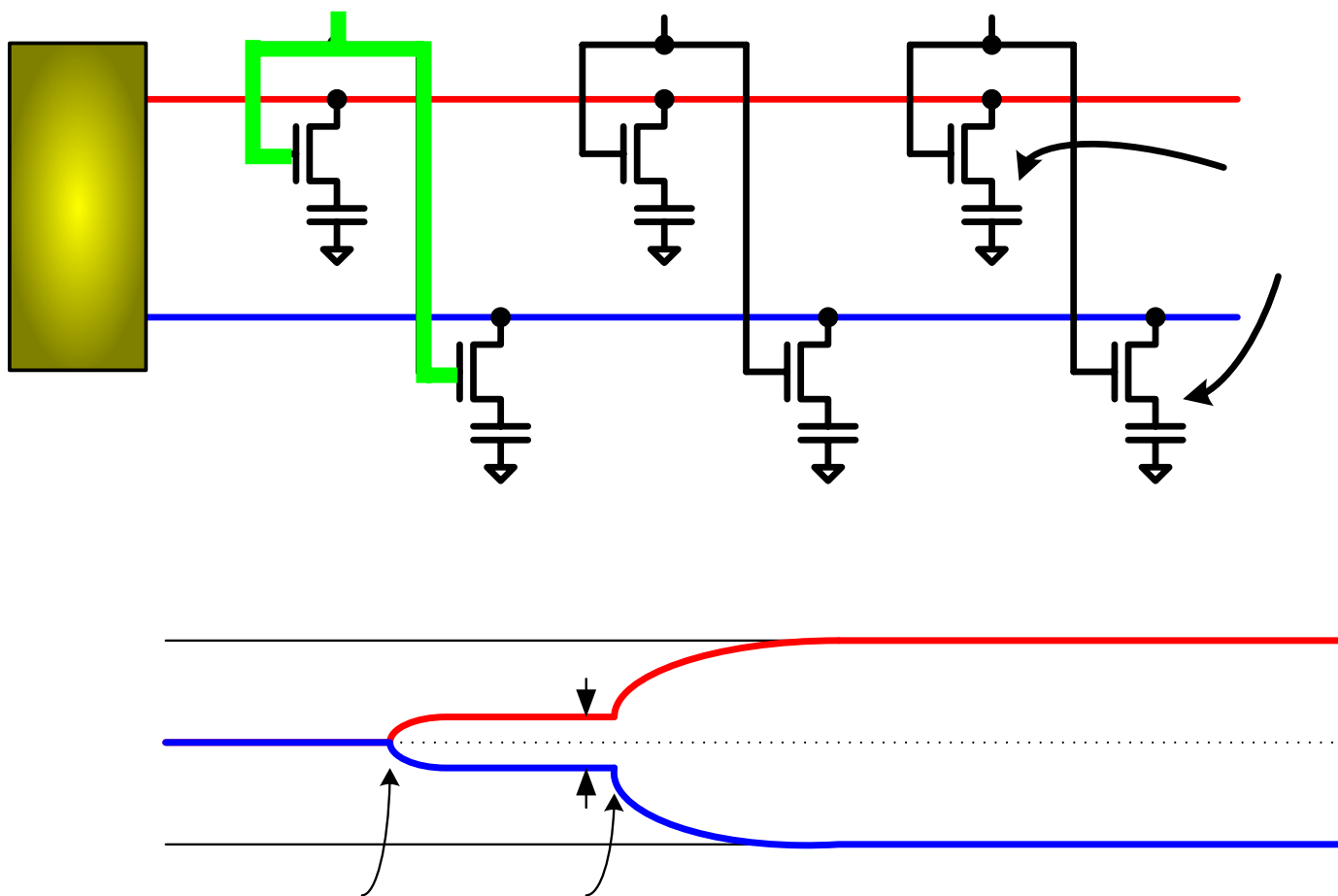


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The "2T" Architecture



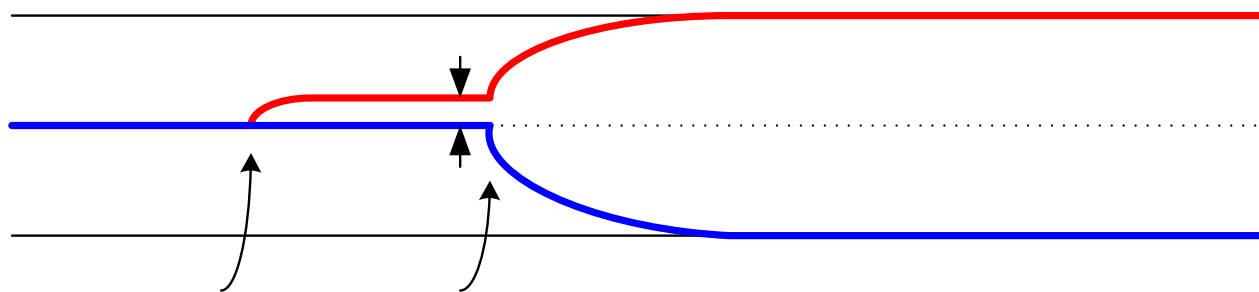
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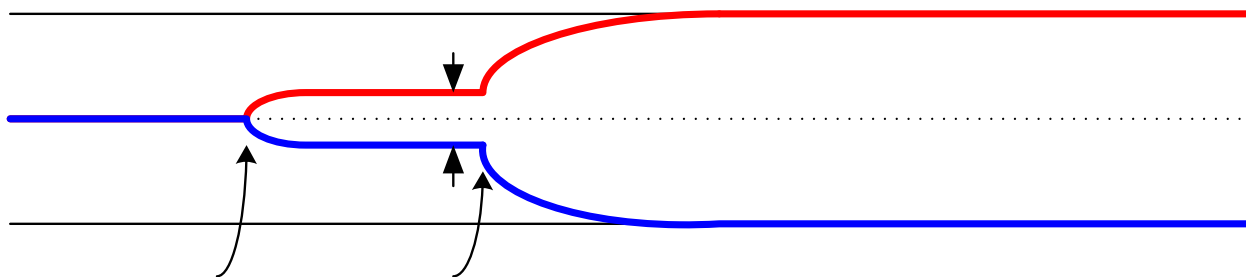
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Sensing Comparison

1T



2T

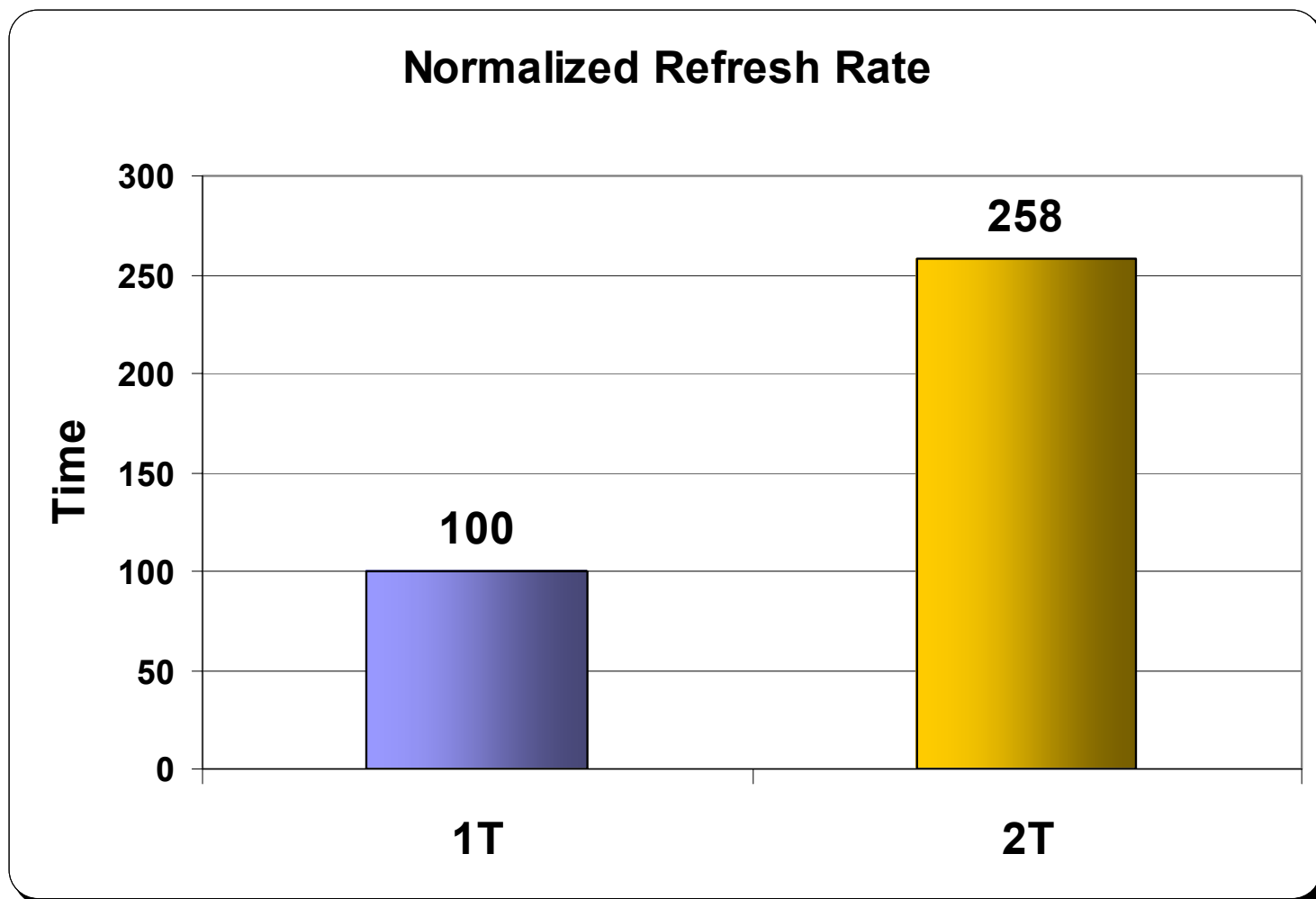


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Refresh Rate “1T” vs “2T”

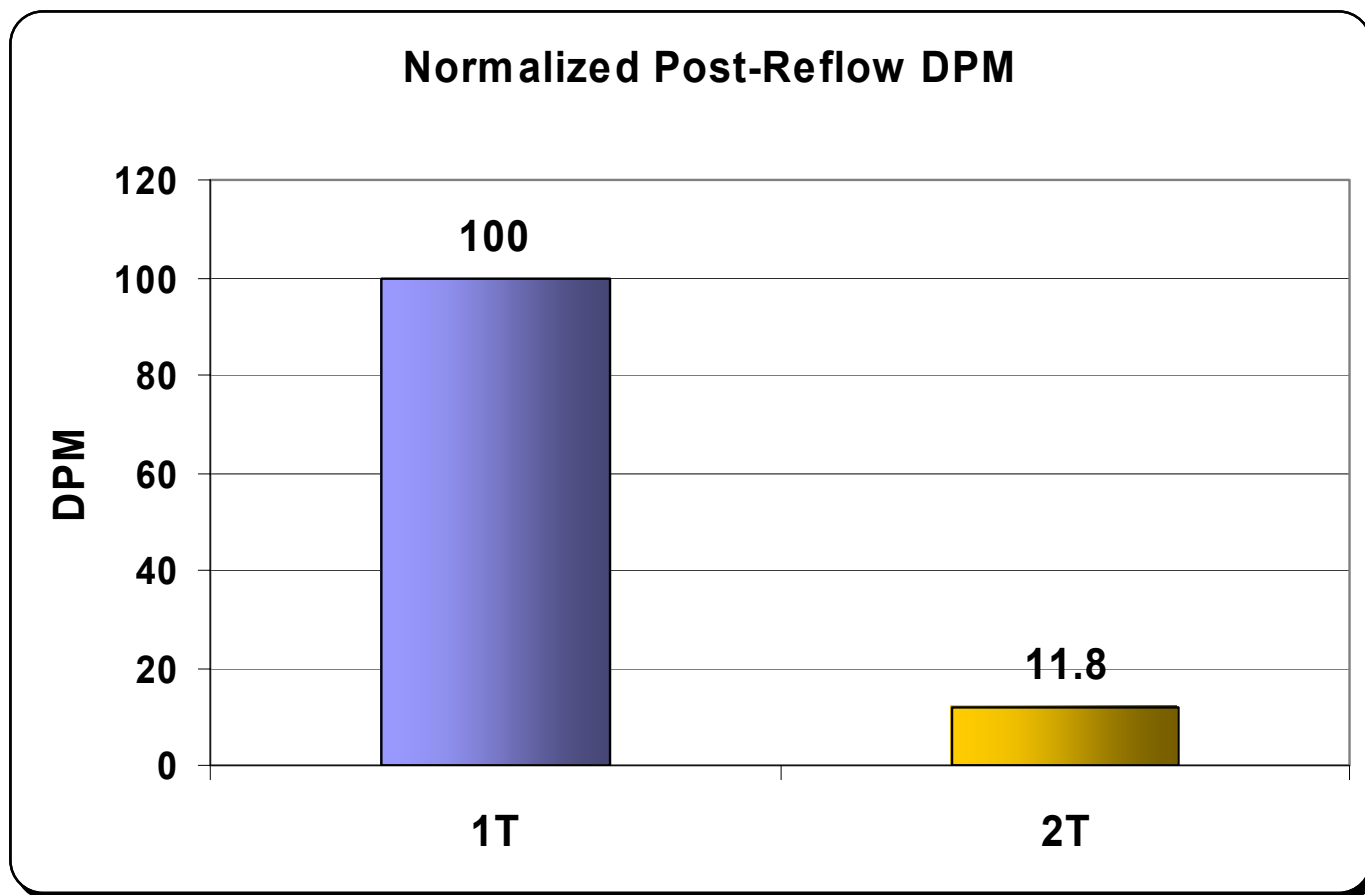


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Post-Reflow Normalized DPM “1T” vs “2T”



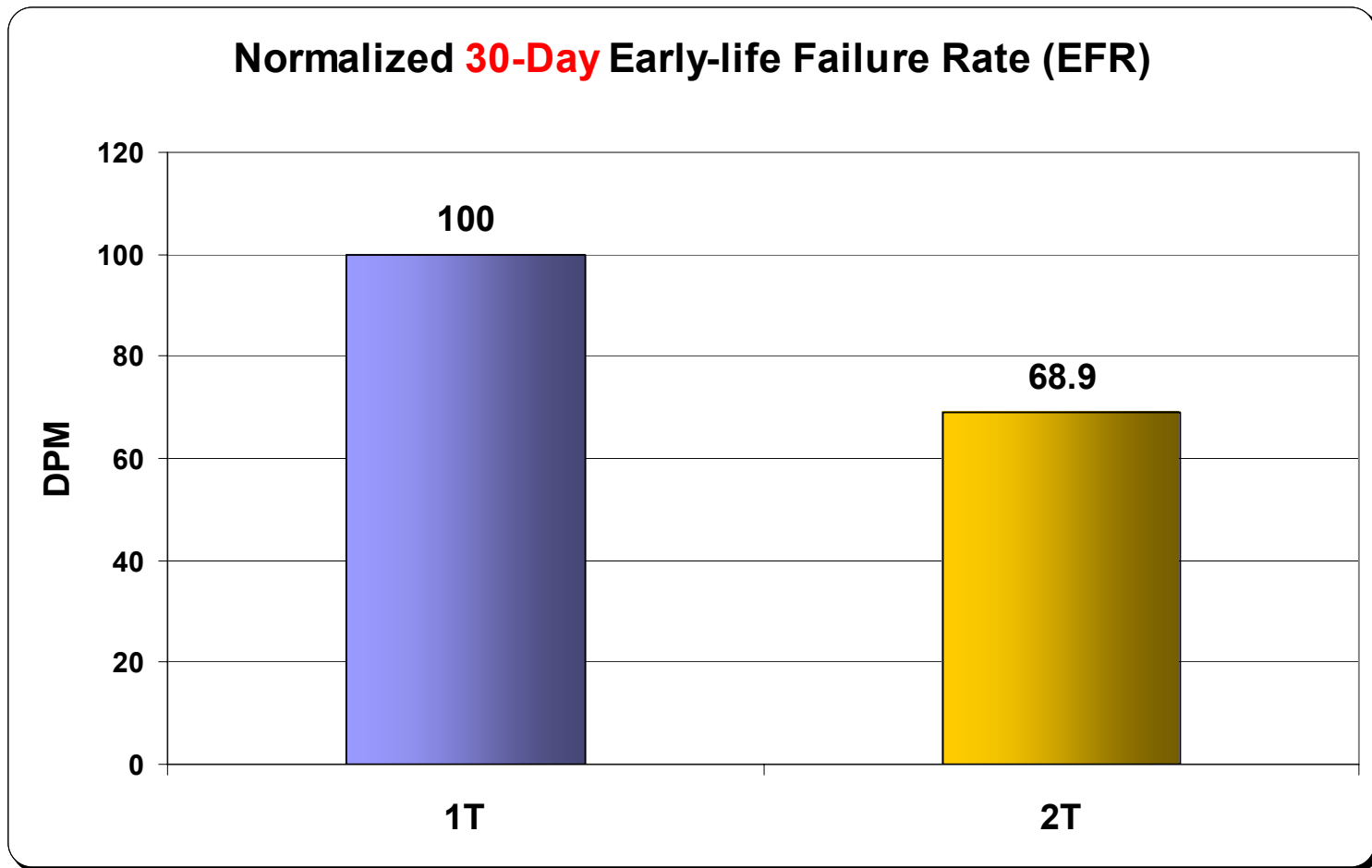
Procedure:

Fully tested devices subjected to 3X convection reflow, then tested again for degradation

Conditions:

3X convection reflow at 260°C

30-Day Early-life Failure Rate (EFR) “1T” vs “2T”

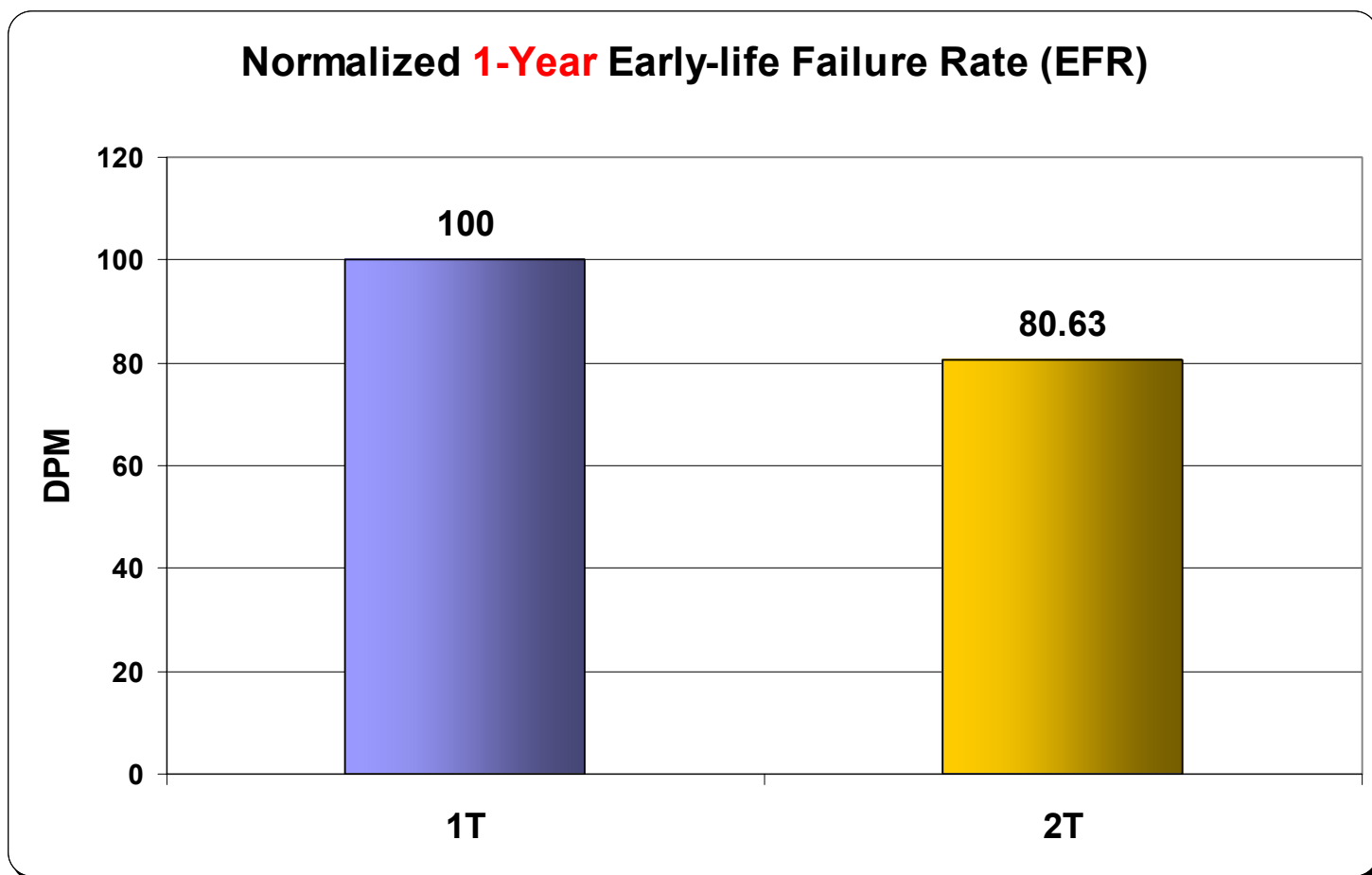


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1-Year Early-life Failure Rate (EFR) “1T” vs “2T”

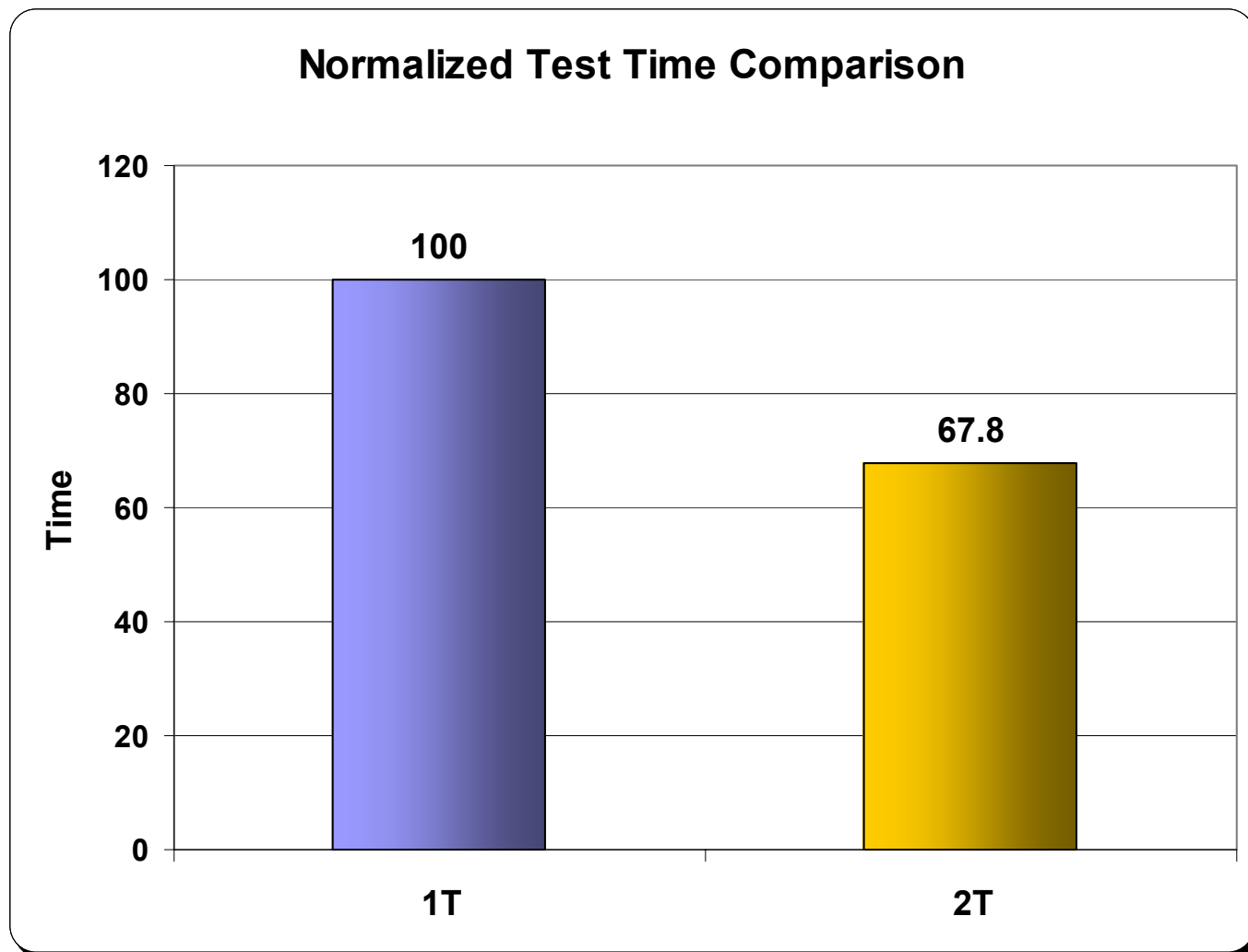


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Test Time “1T” vs “2T”



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“1T” vs. “2T” – Other Benefits and Tradeoffs

- Increased sensing margin allows for reduced array access cycle times
 - Lends itself nicely to Pseudo-SRAM
- Better refresh characteristics provide lower power consumption for mobile applications.
- Die Size Increase
 - Not as substantial at lower densities
 - Further offset at smaller geometries that may be pad-limited.

Summary

- The “2T” architecture is well suited for low-density, KGD DRAM products requiring extended performance and high wafer level quality and reliability.