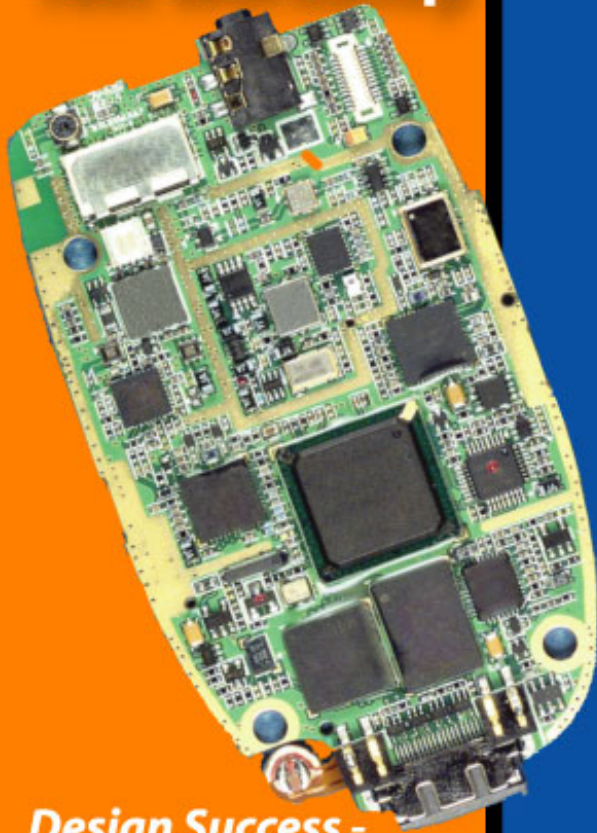


12th Annual

KGD

**Packaging &
Test Workshop**



*Design Success -
KGD Starts
at the Beginning*

Sept. 11-14, 2005 , Napa, CA

International Rectifier
Known Good Die - The SureCHIP™ Process

Rick Pierson
Manager, Die Sales Business Development
International Rectifier

International
IOR Rectifier

DIE PRODUCTS

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What is KGD?

Known – How is it known?

Good – To what spec or level is it good?

Die – It's Die, but is this still in wafer form
and what happens when you do Die saw?

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The Standards for KGD

- There are standards for KGD, but what if you screen to a higher level than the standard?
 - Does it become BTKGD (Better Than Known Good Die)??
 - Why would you want to screen higher than KGD?
- The standards offer a certain level of integrity but this level may not be appropriate for users application
- KGD suggests an ultimate level of integrity, but it isn't. If it were, every-time someone identified a way of improving the Die integrity, the the KGD spec would need to change

KGD – The Right “Fit” for Users?

- The fact is that KGD is open to interpretation
- Users desire Die that are the right ‘Fit’ for their application
 - ‘Fit’ meaning to meet users
 - Electrical
 - Specifications
 - Reliability Concerns
 - Connectivity Issues
 - Mechanical
 - Size Challenges / Constraints
 - Visual Requirements
 - And of course, *PRICE*
- All these factors need to be aligned for the Die to become the right ‘Fit’ for the user and his/her application

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Better Descriptions?

- GED - Good Enough Die
- BAD - Barely Acceptable Die
- DAFA - Die Appropriate for the Application

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L.A.T.

Lot Acceptance Testing for Power Devices

– Advantages

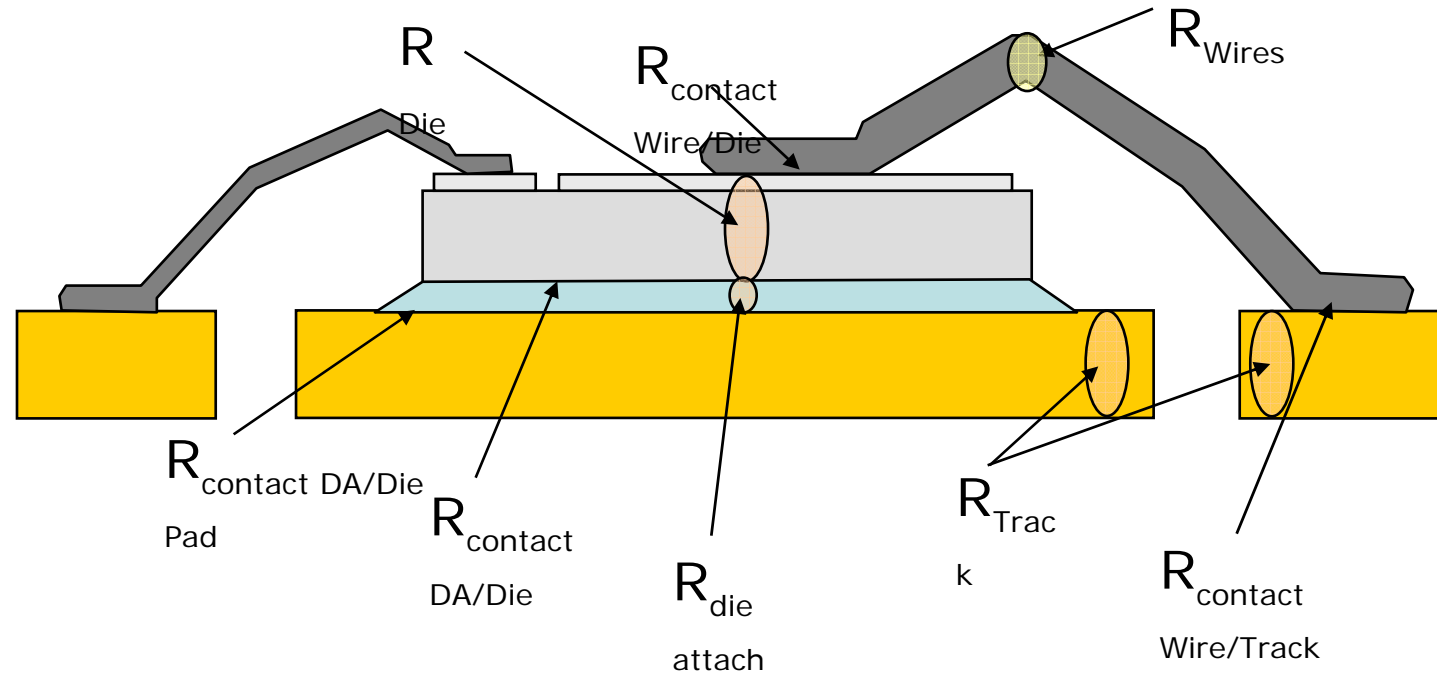
- Can screen samples of a device to customer's full specification
- Easier to handle

– Dis-advantages

- Only sample tested to full parameters
- Validity of package, bonding, die attached used compared to end users application (especially an issue for Power Die)
- Logistics difficult to manage

L.A.T. How Applicable for Power Die?

- Possible differences compared with end application (looking at one parameter as an example)
 - R_{track} , $R_{\text{Die attach}}$, R_{contact} , $R_{\text{contact DA/Die}}$, $R_{\text{contact DA/Die pad}}$ and R_{wires}
 - So how applicable will measurement be to end application?

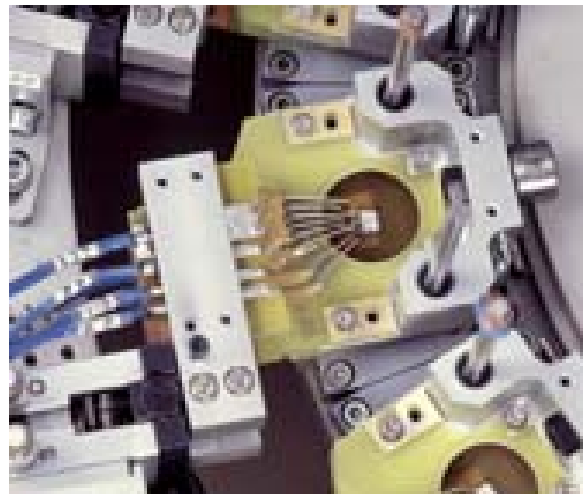


Burn-In for Power Die

- IR Does not burn in Die
- For our Power devices we see very limited parametric shift, so we don't feel it necessary to burn-in Die

SureCHIP™ - The ultimate in Die Integrity?

- Testing carried out on singulated Die
- Testing to 'virtually' package part limits
- 100% visual inspection after wafer saw

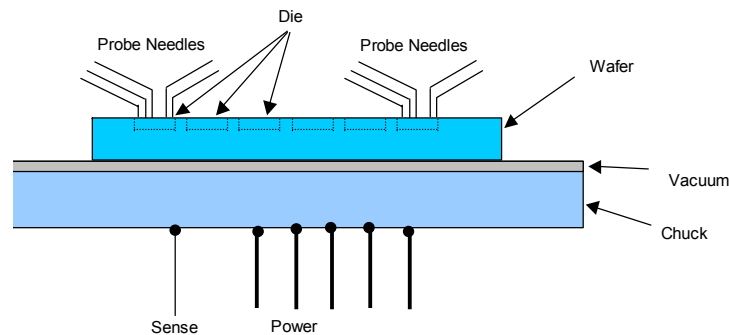


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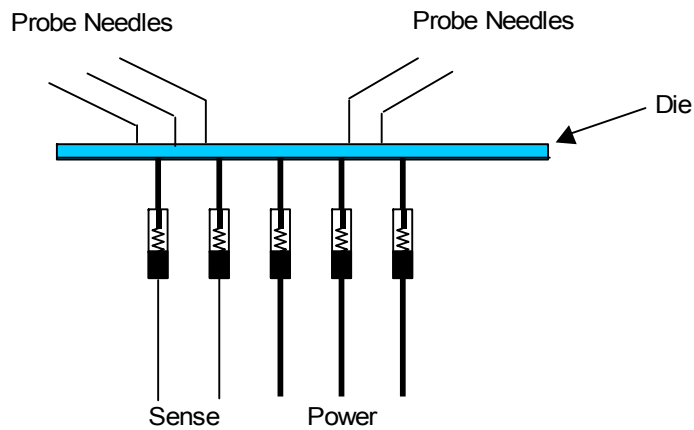
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Limitations With Wafer Probe



- Multiple contacts between backside of wafer and chuck tester
- Die to die interference cannot be isolated
- Parallel testing resulting in multiple signal paths that can effect results
- Key measurements impacted by Kelvin contacts over entire backside of wafer
- $R_{ds(on)}$ accurate down to $20m\Omega$
- I_d constrained to less than 10A
- Higher risk for final application due to dicing operation

IR's SureCHIP™ KGD Process



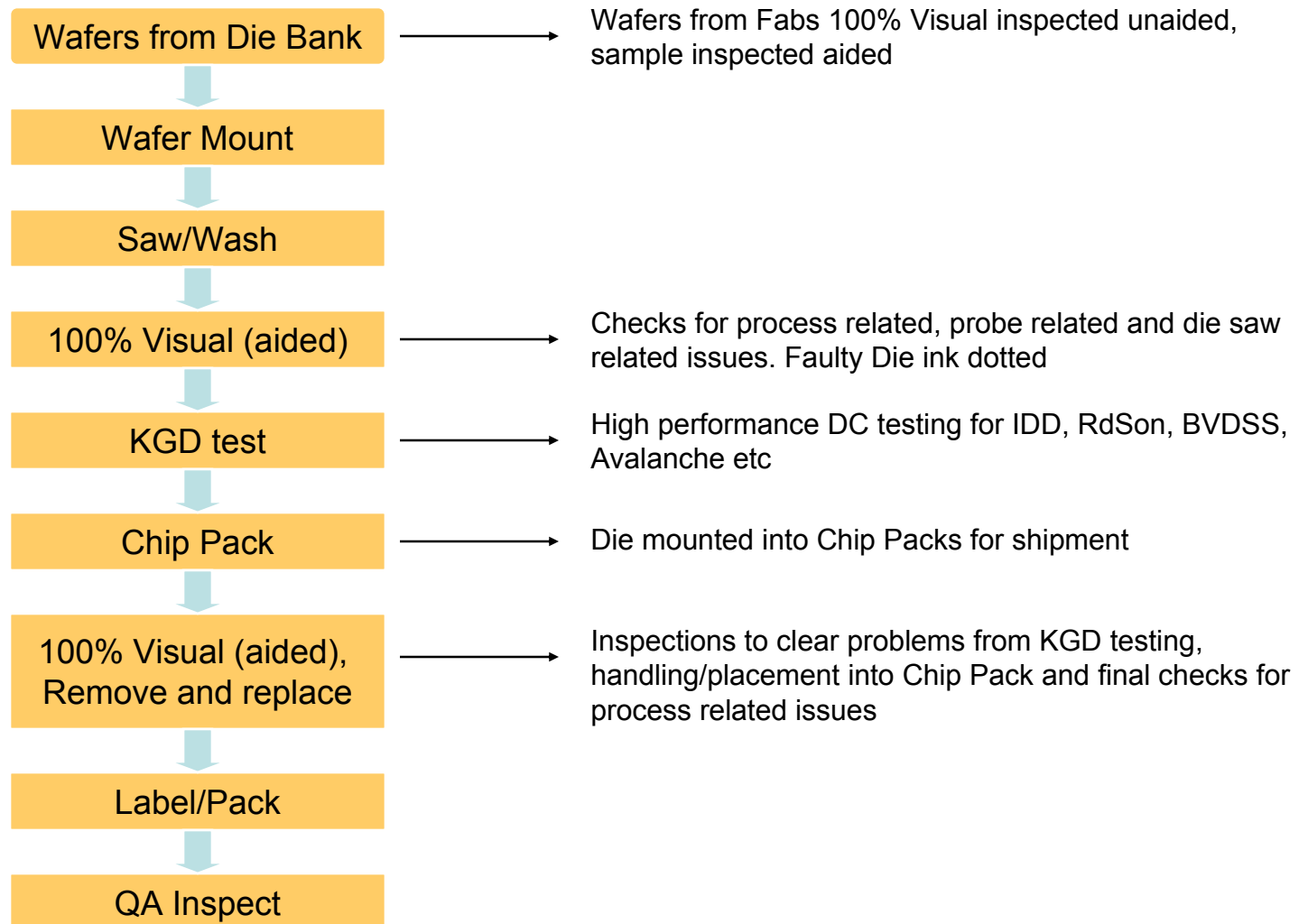
- ✚ Hybrid modifications provide uniform contact
- ✚ Direct contact with isolated Die
- ✚ Singulated testing, eliminating lateral current paths
- ✚ Hybrid modifications enable cleaner noise environment
- ✚ Kelvin contact fixed to single location for single die
- ✚ $R_{ds(on)}$ accurate down to $2.5m\Omega$
- ✚ I_d possible above 75A
- ✚ Singulated Die pre-screened for mechanical defects

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SureChip™ Process Flow



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SureCHIP™ Test Set-Up

3 test generators perform the testing
Low Voltage Generator for testing
Rdson, Vf, Vsd, Vceon, Vdson, etc

High Voltage Generator for testing
BVdss, Idss, Igss, Vr, etc
UIS Generator for Avalanche

Tests are carried out on Die mounted into a test nest



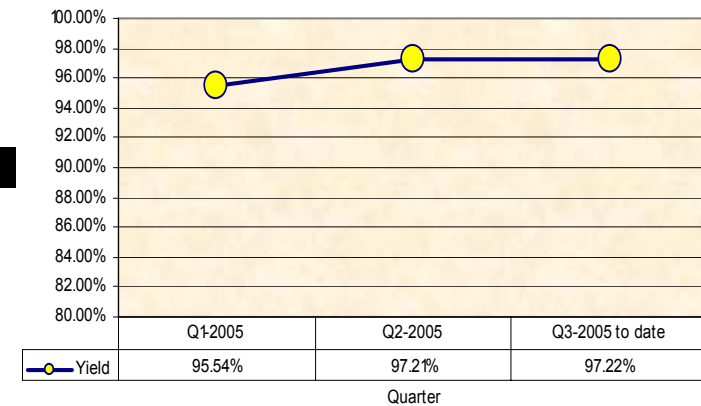
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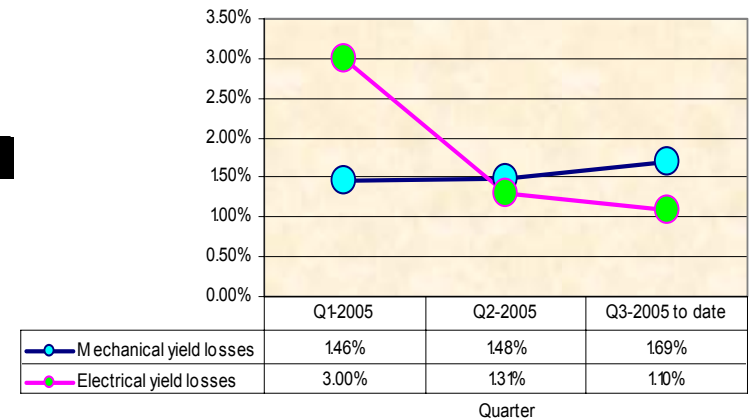
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Yield Performance

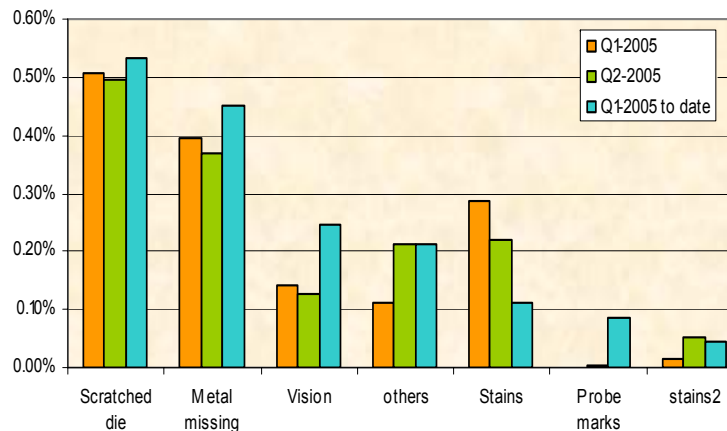
Yield (KGD)



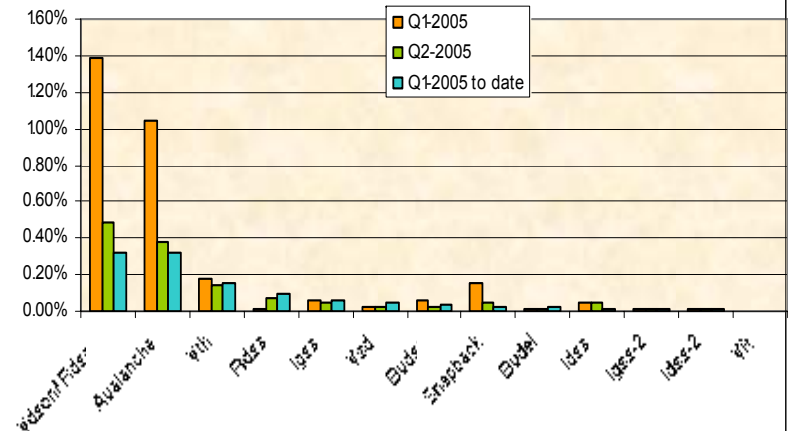
First pareto for KGD



Mechanical yield losses pareto



Electrical yield losses pareto



SureCHIP™ Cost Analysis

- There are 5 main factors affecting the decision to utilize SureCHIP™ for a given application
 - The bare die size/cost
 - Substrate cost
 - # of Die/module
 - Module test cost
 - Wafer saw/visual inspection cost and yield loss

SureCHIP™ Cost Benefit Analysis

Figures used are only an example. Please consultant
 BM/Die Sales for devices pricing and customer for
 module info

Current situation

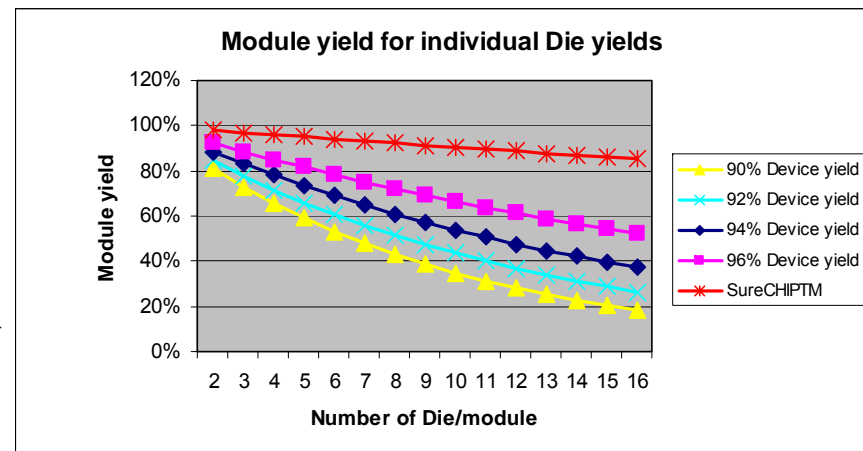
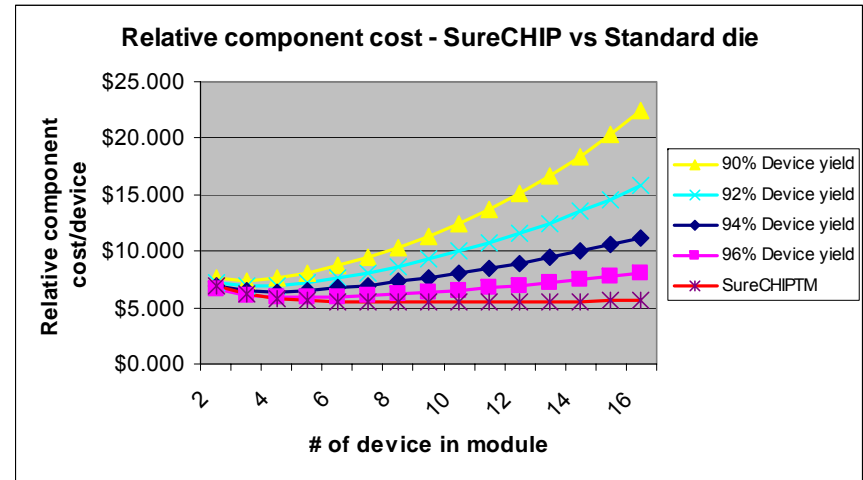
Current Die price	\$3.88
# in module	7
Component price/module	\$27.16
Substrate cost	\$2.00
Assembly cost	\$1.50
Test cost	\$1.00
total cost/module	\$31.66
Module/substrate yield	83%
Effective cost/module	\$38.14
Effective component cost	\$5.45

SureCHIP™ Solution

IR SureCHIP™ solution cost	\$4.50
# in module	7
Component price/module	\$31.50
Substrate cost	\$2.00
Assembly cost	\$1.50
Test cost	\$1.00
total cost/module	\$36.00
Module/substrate yield	97%
Effective cost/module	\$37.11
Effective component cost of SureCHIP™ solution	\$5.30

Additional Benefits

Die visually inspected after saw eliminating this yield fallout at customer
 Potentially less system test cost due to higher level of die testing



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Additional Benefits

- Eliminates customer yield loss after saw
- No cost for visual inspection after saw
- Clearer separation of responsibilities

That being said, the performance in the customer's system will ultimately depend upon their die attach, bonding and assembly processes

Conclusions

- The SureCHIP™ process does assure a high level of integrity
 - Higher Performance Testing
 - More Accurate Testing
 - Visual Inspection After Wafer Saw
- Cost/Benefits analysis needs to be done for each requirement to determine if it is the right “fit” for the application