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# ***Solder Selections for Stacked Die and Low Temp Applications***

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2006 KGD Packaging  
& Test Workshop  
Sept. 10-13, 2006  
Napa, California

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# The Chip Scale Advantage

- *Minimizes mechanical damage*
- *Thermal limitations – need for low temperate solutions (sub 150C alloys)*
- *Real estate - small footprint and 3D*
- *Proto die builds (especially FIBs)*
- *Quick turn package/assembly solutions*
- *Lead Free (InSnAg, InSn, InAg, etc)*
- *Conductive epoxy does not work well*

# Must Satisfy the “MEE” Requirement

What is “MEE”? MEE are the basic reliability factors plus a cost requirement that includes:

- Mechanical durability
- Electrical requirements
- Economically feasible

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# Economics

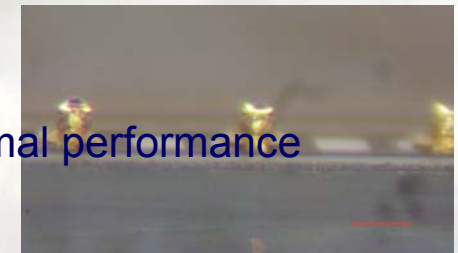
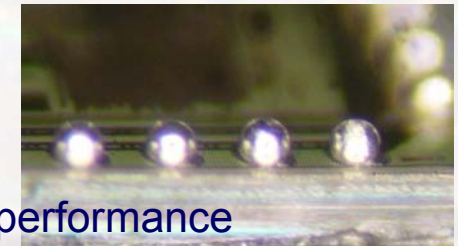
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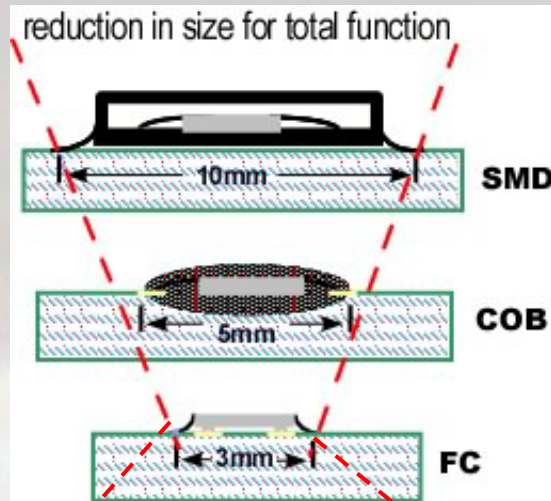
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# Die Stacking Techniques

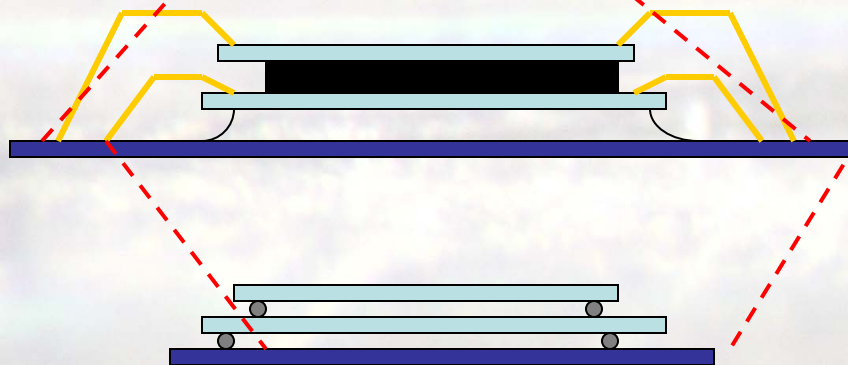
- Wire bond
  - Requires die attach
  - Cost of wire
  - Can be a reliability concern
  - Wires can lead to marginal electrical performance and mechanical damage.
  - No thermal advantage except at the die attach.
  - Cost proportional to yield and number of wire bonds
- Flip chip bumps
  - Uses standard SMT equipment
  - Limited reflows due to allow selections
  - Cost is reflective of pitch and bump size
  - Good electrical, mechanical and thermal performance
- Au and Cu stud bumps
  - Not practical for high pin count device
  - Can damage die
  - Excellent electrical, mechanical and thermal performance
- Pillars
  - Good for small pitch and high I/O
  - Costly



# Reduction in Size; Reduction in Cost



Courtesy  
www.DPC.org



Solder bumping is the correct path towards package size direction:

- Process and Product design rules can be a hindrance on package shrinks
- Designs that require more board real estate and process equipment should be avoided
- Avoid processes that require thicker package due to design rules and assembly needs
- Incorrect die to die bonding can reduce yield and profit margins
- Bumps demonstrate an improvement in size, process and performance

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# Die Stacking – Why Wire Bonds

*No standard footprint for all the possible pad I/O layouts – even within the same company.*

- Wire bonds increase package thickness with wire sweep and die attach
- Wire bonds also can require minimum wafer thickness
- The math.....125um loop compared to a post reflow bump at 65 to 70um. Bump stacking 4 die could save 150um (6 mils)
- Overmold requirements for wire sweep can increase x, y and z dimension of the package even in leadless packages.

# Improving the Process - Stacking with Diverse Solder Alloys

- Limits to stacking are due to the number of qualified bump alloys and reflow temperatures.
- Having alloys with liquidus and solidus temperatures that do not overlap provide expanded stacking capabilities
- Solders must have reflow profiles that do not damage the die or substrate materials
- Alloys and the corresponding bumping technique must be cost effective
- An additional Christmas present would be to be able to stack with multiple bump sizes

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# Mechanical

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# How Stack Die More Reliability

Avoid techniques that can lead to reliability concerns:

- CTE mismatch of components
  - Bumping limits contact area so CTE mismatch not as critical
  - Bumps can be placed strategically and “redistributed”
- Mechanical damage to the die
  - Wire bonding
  - Wire bonding on unsupported structures
- Electrical degradation
  - Cross talk, inductive coupling and transmission lines

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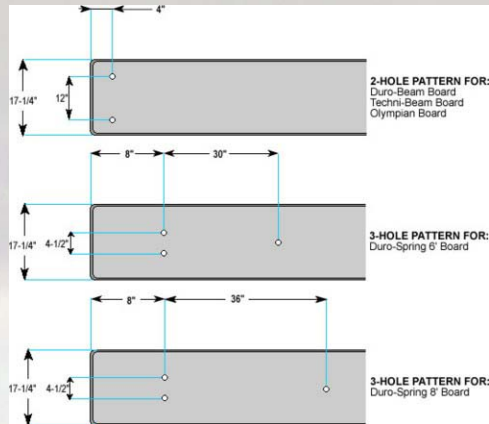
# Wire Selection

- Premier wire to prevent problems with sagging and swaying, loop height variability and neck breakage/variation
  - Must maintain loop height variation over long wire distances
  - Linearity – maintain lateral wire straightness
  - Wire clearance – leakage and cross talk
- This is prior to overmold

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# Wire Bonding on Overhanging Stacked Die

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[Now you have a pool with a diving board. What are your reliability commitments to your customers.](#)

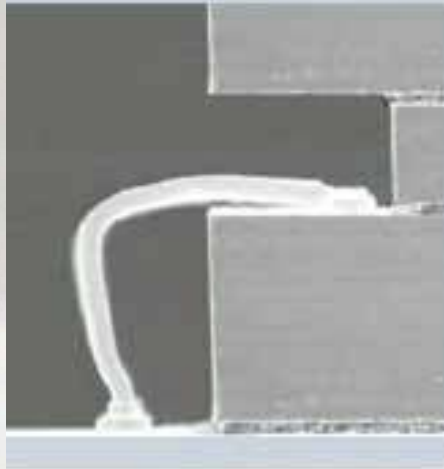
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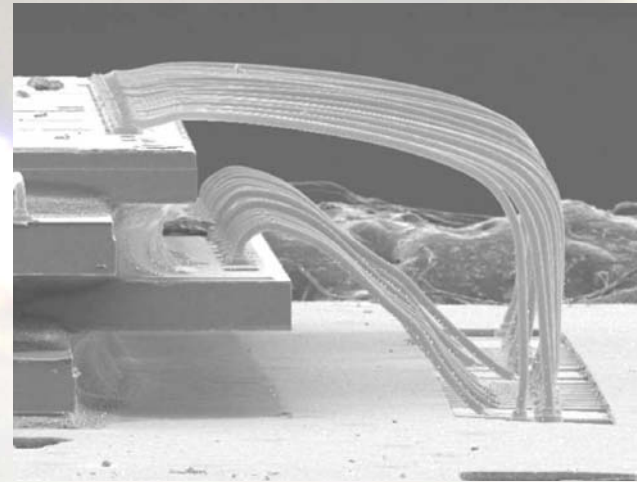
# Good and Bad Wire Bonds

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KNS

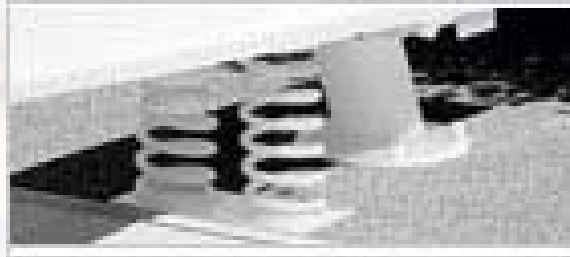


Wire bonded on rigid surface – good idea

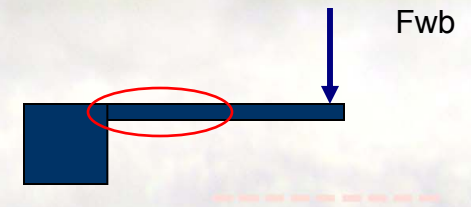
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Wire bonded on rigid surface – scary idea



Brittle materials don't like  
tensile stresses



# Best Technique – Use Bumps

When possible use solder bumps:

- Might require interposers
- Might require stacking prior to final assembly

But:

- Faster speed
- Minimized inductance
- No transmission lines
- Higher package density
- Heat transfer is better

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# Alloy Selection

- Eutectic materials are best
- Large delta between liquid and solid is not good
- Pay special attention to adding an alloy that can cause a drop in temperature (Bi, Sb)
- Sn and Au have two eutectic points
- In and Au have 4 (but only 1 is in the range of typical processes)
- Make sure the solidus does not overlap the liquidus of another alloy
- Keep the system to two alloys if possible

# Problem Alloys Eliminated

- Bi,
- Sb
- Zn
- Cd
- Pure Sn
- These materials can lead to sharp drops in liquidus, brittle solders, poor mechanical properties, or environmental issues
- Alloy with a temp delta  $>30\text{C}$  between liquid and solid

# Solder Selection & Design Rules

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Bi lowers the liquidus temperature but will degrade the fatigue life.

Zn and indium (In) additions improves the tensile strength but the fatigue life degrades

Indium additions lower the melting temperature

Dissolution of Au into In is slower than Sn-Au

The lower solubility of Au atoms in the In-Sn solder prevents Au-embrittlement

In and Sn alloys wet Au.

This AuIn interface IMC acts as a diffusion barrier and prohibited the formation of AuSn<sub>4</sub> in the solder matrix

Soft alloys coin. (Stud bumps are harder and coining can damage lowk/BOAC components)

In based alloys can be used as **lead-free replacements.**

InSnAg has similar properties and thermal profile as SnPb.

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# In - Solutions

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TEMP		Elemental Composition (% by Mass)						TCE
Liquidus	Solidus							@ 20°C
°C	°C							PPM/°C
118	E 118	52	In	48	Sn			20
130		40	In	40	Sn	20	Pb	
143.3	E 143.3	97	In	3	Ag			22
151		90	In	10	Sn			
154		80	In	15	Pb	5	Ag	28
175		70	In	30	Pb			28
181		60	In	40	Pb			27
195		58	In	39	Pb	3	Ag	
210		50	In	50	Pb			27

# The Indium Solution

*When deciding on an alloy one needs to evaluate the following:*

*Strength*

*Solder migration*

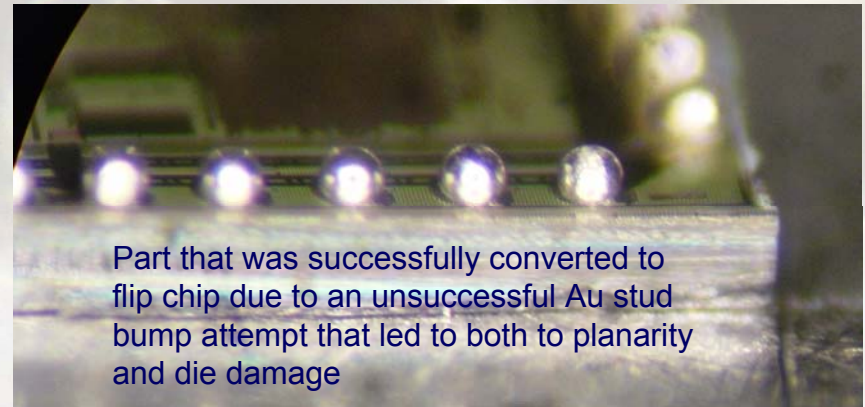
*Creep*

*Thermal Expansion*

*Stress*

*Fatigue*

*Liquidus Temperature*



*Low melting point soft solders such as Indium and its alloys help reduce stress due to CTE mismatch.*

*They exhibit low yield stress but are subject to creep over time.*

# Pb - Solutions

TEMP		Elemental Composition (% by Mass)							TCE
Liquidus	Solidus								@ 20°C
275	260	81	Pb	19	In				27
296	287	92.5	Pb	5	Sn	2.5	Ag		29
302	275	90	Pb	10	Sn				29
302	275	89.5	Pb	10.5	Sn				29
303	E 303	97.5	Pb	2.5	Ag				
304	299	95.5	Pb	2.5	Ag	2	Sn		
309	E 309	97.5	Pb	1.5	Ag	1	Sn		30
310	290	90	Pb	5	In	5	Ag		27
310	300	92.5	Pb	5	In	2.5	Ag		25
312	308	95	Pb	5	Sn				30
313	300	95	Pb	5	In				29
313	E 313	91	Pb	4	Sn	4	Ag	In	
290	267	88	Pb	10	Sn	2	Ag		29

# Sn - Alloys

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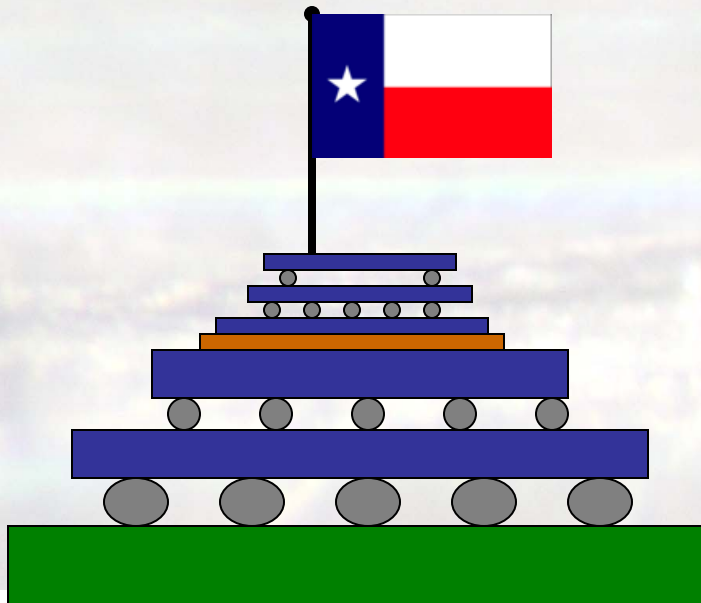
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TEMP		Elemental Composition (% by Mass)						TCE
Liquidus	Solidus						@ 20°C	
167	154	70	Sn	18	Pb	12	In	24
179	E 179	62.5	Sn	36.1	Pb	1.4	Ag	27
183	E 183	63	Sn	37	Pb			25
183.3	182.7	62	Sn	38	Pb			
186	183	70	Sn	30	Pb			22
187	175	77.2	Sn	20	In	2.8	Ag	28
189	179	61.5	Sn	35.5	Pb	3	Ag	
191	183	60	Sn	40	Pb			25
205	183	85	Sn	15	Pb			
205	204	86.9	Sn	10	In	3.1	Ag	
212	183	50	Sn	50	Pb			23
217	E 217	90	Sn	10	Au			
221	E 221	96.5	Sn	3.5	Ag			30
227	E 227	99	Sn	1	Cu			
227	E 227	99.3	Sn	0.7	Cu			
182	178	62.6	Sn	37	Pb	.4	Ag	
220	217	95.5	Sn	3.9	Ag	0.6	Cu	
280	E 280	80	Au	20	Sn			16

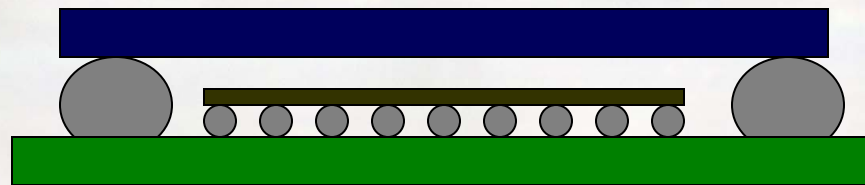
# Building a Better Die Stack

- Decide on how many layers and the sequence of assembly
- Allow for heat spreaders
- Overcome the unknown
- Prebumped substrate
  - 92.5Pb5Sn2.5Ag
  - (296C/287C)
- First die attach to substrate
  - No bumps, pads only; first assembly reflow
- Standard Pb-Free die
  - 96.5Sn3.5Ag
  - (221C eutectic)
- Assemble Cu heat spreader and dual die
  - 63Sn37Pb
  - (183C eutectic)
- Controller assembly
  - 97In3Ag
  - (143C eutectic)
- Plant Flag



# Stacking with Multiple Bump Sizes

Multiple bump sizes provide nesting as well as an additional path z-level integration.



**Substrate**

**Reflow Pb-free (SnCuAg) Die**

**Reflow SnPb die**

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# Electrical

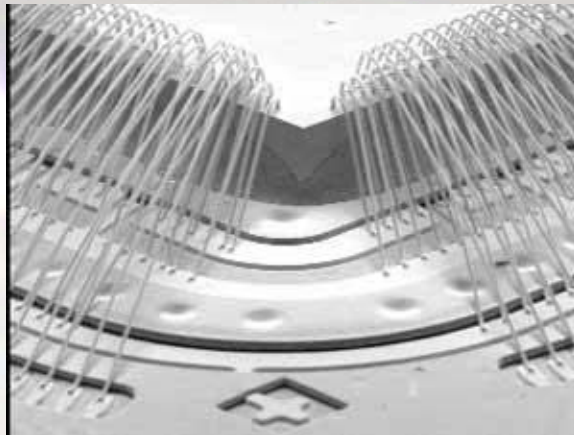
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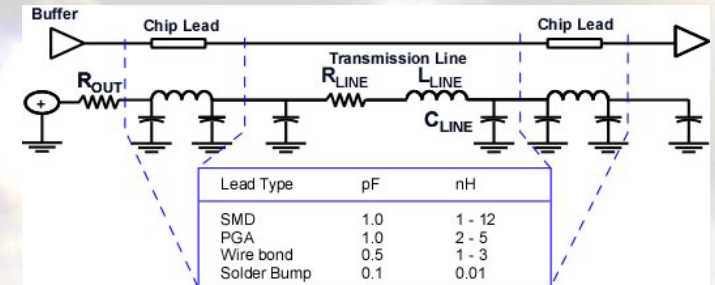
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# All that Cross Talk

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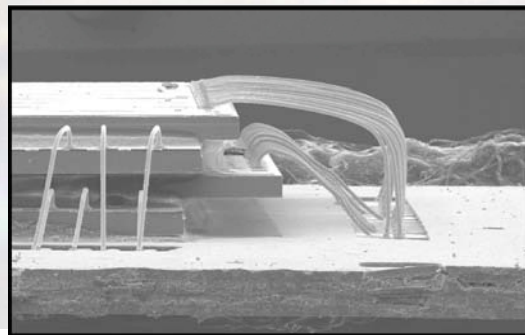


Courtesy KNS



Courtesy DPC

- The more wire the more transmission lines.
- The more transmission lines the more cross talk
- The more of items 1 and 2, the worse the yield



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# Folded Flex Stacking

- Flex temperature limitations
- CTE mismatch between solder, flex and substrate
- Rigid solders don't like to be folded
- In based materials are much more forgiving than Sn solders
- Au and copper studs can be damaging to the flex and die

# Solder Bumps Communicate Faster

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Shorter Signal Distance

Lower contact Resistance (CRES)

Metals have better conductivity and don't degrade like epoxies

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# Summary

- Die can be stacked using flip chip bumps when the proper alloy is selected
- Bumping satisfies the “MEE” requirement
- A number of Indium, Tin and Lead alloys have liquidus/solidus temperatures that do not overlap
- Electrical performance can be improved with bumps
- Integrated solutions with wire bonds are an option
- Multiple bumps sizes are also an option



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**Thanks for  
your time.**

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